



AXVM2152 Development Board User Manual

Alinx Electronic Limited
www.en.alinx.com



Document Revision History

Section	Revision Summary
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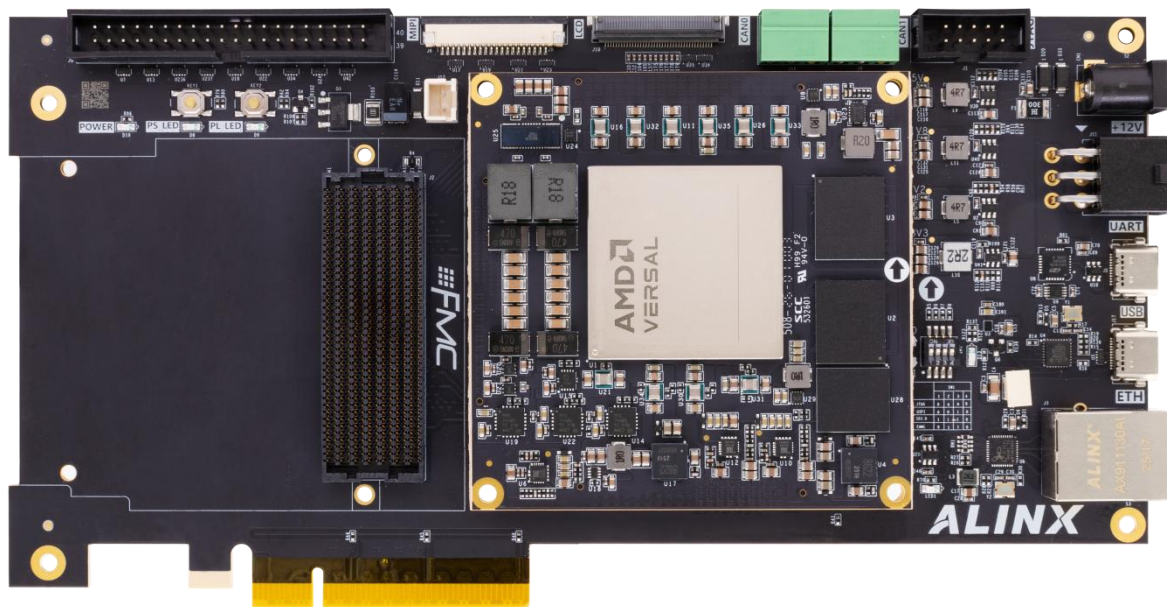
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Alinx Electronic Limited has officially released its AMD FPGA Versal Prime development platform (model: AXVM2152). To help you quickly understand this development platform, we have compiled this user manual.

This Versal AI Edge development platform adopts a SoM plus carrier board model, facilitating secondary development and utilization of the SoM by users. The carrier board design includes one FMC+ interface , two CANFD communication interfaces, one MIPI camera interface, one PS Gigabit Ethernet interface, one PS UART interface , one PS USB HOST interface, one 40-pin FPC interface, one 40-pin expansion port, and interfaces supporting PCIe Gen5.0/4.0 . It meets the requirements of users for various high-speed data exchange, data storage, video transmission and processing, deep learning, artificial intelligence, and industrial control, making it a "professional-grade" development platform. It provides possibilities for high-speed data transmission and AI applications , as well as the early verification and later application of data processing. This product is believed to be very suitable for students, engineers, and other groups engaged in FPGA development.



Chapter1 Development Board Introduction

Here is a brief introduction to the features of the AMD FPGA Versal Prime AXVM2152 platform.

The development board's overall structure follows our established SoM + carrier board design. High-speed inter-board connectors connect the SoM and carrier board.

The SoM mainly consists of a Versal Prime XCVM2152 , two LP DDR5 memory modules , one QSPI FLASH, and one eMMC. We selected the Versal Prime Series XCVM2152 chip, packaged in an NFVM1369 package. The XCVM2152 and LP DDR5 have a 32- bit data bus width , with the LP DDR5 having a capacity of up to 4 GB and a data rate of 8533 Mbps, meeting the high buffer requirements during data processing. Additionally, the SoM has a 32GB eMMC and 128MB QSPI FLASH for system startup and data storage. The carrier board features a rich array of peripheral interfaces. The following diagram shows the overall structure of the AXVM2152 platform:

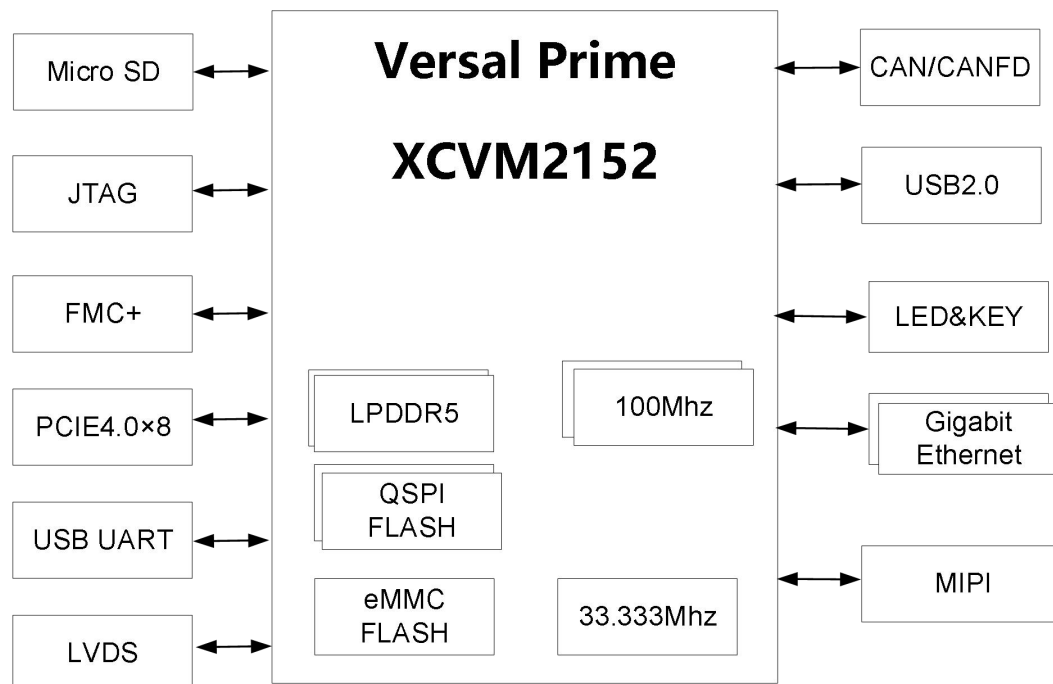


Figure 1.1.1 - Schematic diagram of the development system structure

This diagram shows the interfaces and functions that our development platform can contain.

- AMD Versal Prime chip XCVM2152 - NFVM1369 .
- eMMC: The development board comes with a large-capacity 32 GB high-speed eMMC memory (model MTFC32GAPALBH-IT). It can be used for FPGA firmware and user data storage , etc.
- Two LPDDR5 SDRAM modules with 32-bit data width, offering a total capacity of up to 4 GB.
- QSPI FLASH: Two 64MB QSPI FLASH memory chips, designed for storing FPGA configuration files and user data.

- The PCIE x8 interface supports PCIe Gen4.0x8 or Gen5.0x4, meeting the requirements for high-speed expansion, high-performance computing, and high-speed storage expansion.
- CAN Communication Interface: Features two CAN/CAN FD bus interfaces, utilizing TI's TJA1051T chip with 3-pin green terminal blocks.
- USB UART Interface: A single UART-to-USB converter for computer communication, facilitating user debugging. The serial chip employs the Silicon Labs CP2102N USB-UART chip, while the USB interface utilizes a Type-C connector.
- USB 2.0 interface: The USB 2.0 interface is connected to the FPGA PS side via the USB3320C control chip, enabling connections for devices such as mice, keyboards, and USB drives. The USB interface utilizes the USB Type-C standard.
- Gigabit Ethernet interface: One 10/100M/1000M Ethernet RJ45 port for Ethernet data transmission with computers or other network devices. The network interface chip employs the JL2121 Ethernet PHY chip to provide users with network communication services.
- FMC+ Interface: A single FMC+ interface providing outputs for LA, HA, HB, and 8 pairs of GTM transceivers, supporting external connection of various XILINX or Alinx FMC modules (including HDMI input/output modules, dual-camera modules, high-speed AD modules, etc.).
- JTAG Debug Port: A single 10-pin, 2.54mm standard JTAG port for FPGA program download and debugging. Users can perform debugging and program download on the FPGA system using the XILINX Downloader.
- Micro SD card slot: A single Micro SD card slot supporting the SD 3.0 protocol, enabling FPGA to read, write, and store data on SD cards.
- MIPI Interface: A single MIPI interface supporting MIPI 4xLane, compatible with ALINX's MIPI camera (AN5020).
- LVDS interface: A single LVDS interface for connecting to the ALINX LVDS display.
- Clock: The SoM features two 100 MHz differential crystal oscillators, providing stable clock signals for both the FPGA system and LPDDR5 memory. Additionally, the carrier board includes a 200 MHz differential crystal oscillator for the LVDS interface and a reserved 156.25 MHz oscillator connected to the high-speed transceiver.
- LED lights: 1 power indicator light; 1 Done configuration indicator light; 2 user indicator lights.
- Buttons: 2 user buttons.

Chapter2 ACVM2152 SoM

2.1 Introduction

The ACVM2152 SoM adopts AMD Versal Prime chip, model XCVM2152-NFVM1369. It features speed grade 2 and an operating temperature range of 0 - 110 °C . This model comes in the NFVM1369 package with 1369 pins and a pin pitch of 1.0 mm. The high-performance SoM developed based on this chip boasts outstanding characteristics including high performance, low latency, edge computing capability and low power consumption, making it suitable for applications such as data centers, video image processing and high-speed data processing.

The SoM is equipped with 2 pieces of Micron MT62F512M32D1DS-023 AIT:E high-speed LPDDR5 SDRAM chips, featuring a 32-bit data width, 4GB capacity and a maximum data rate of 8533 Mbps. In addition, the SoM integrates 32GB eMMC and 128MB QSPI FLASH memory, which are used for boot storage, configuration and system file storage.

On this SoM, the PS side expands 53 MIO pins with 1.8V voltage level standard; the PL side expands 44 IO pins with 3.3V voltage level standard, 192 IO pins with 1.2V voltage level standard, as well as 16 pairs of GTY high-speed RX/TX differential signals. Furthermore, equal-length routing and differential signal processing are implemented for the traces between the FPGA chip and external interfaces. With a compact size of only 80 × 80 mm, the SoM is highly ideal for secondary development.

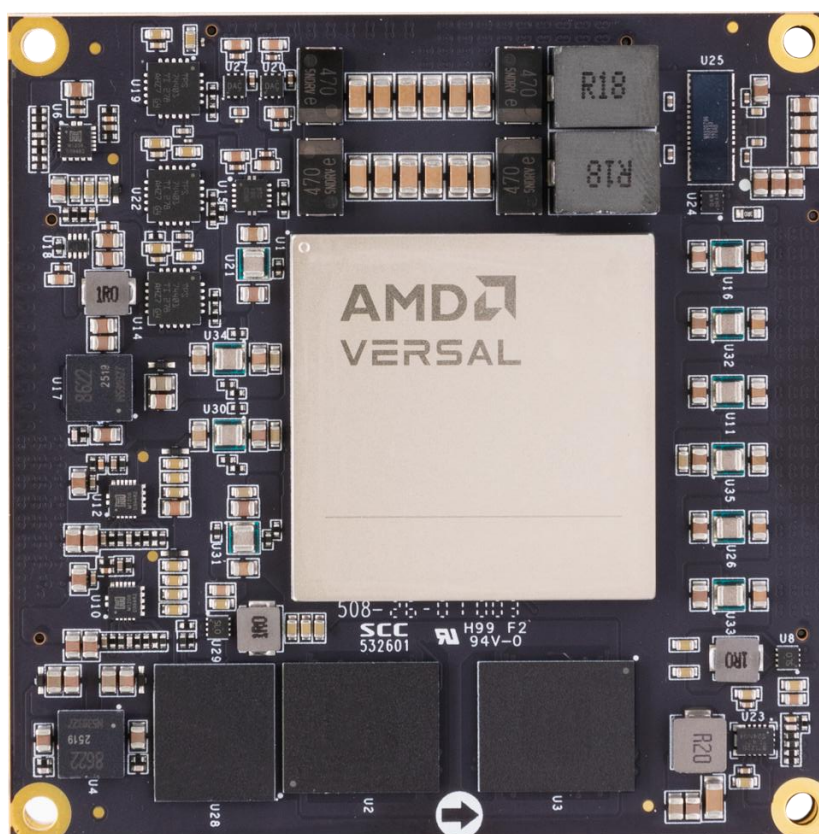


Figure 2.1.1 - Front view of ACVM2152 SoM

2.2 XCVM2152 FPGA Chip

The Versal Prime chip we use is model XCVM2152-NFVM1369, with a speed class of 2, operating temperature range of 0–110 °C, and packaged in the NFVM1369 format. The naming convention for Versal Prime chips is as follows:

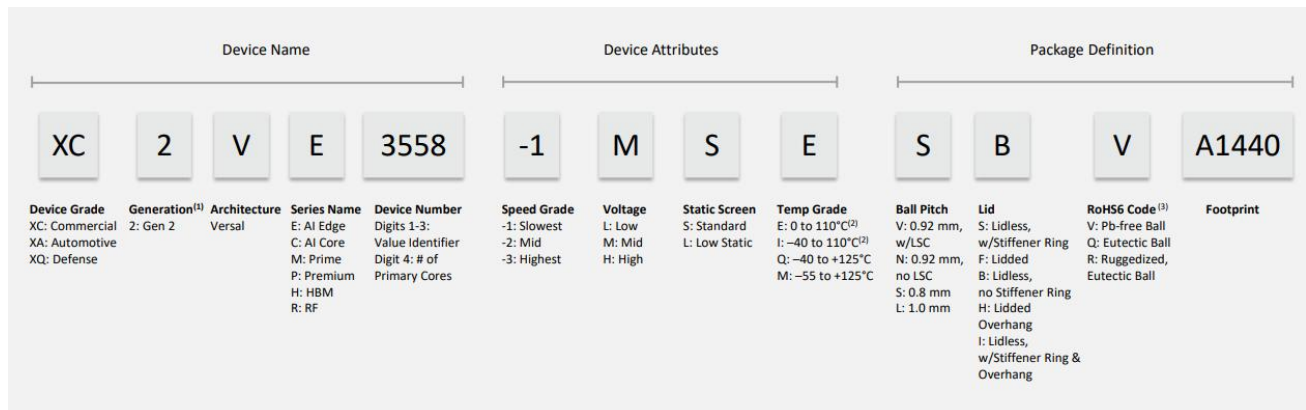


Figure 2.2.1 - FPGA Naming Rules Definition

The main specifications of the FPGA chip XCVM2152 are as follows::

Parameter	Value
Logic Cells	757K
Lookup Tables (CLB LUTs)	346112
Block RAM (Mb) size	27
DSP processing unit (DSP Slices)	1704
PCIe Gen 5x4	2
GT YP	8
GTM	8
Speed level	-2
Temperature rating	0°C-110°C

Table 2.2.1 - Main parameters of XCVM2152

XCVM2152 chip integrates two ARM Cortex™-A 72 processors and two Cortex-R5F processors , along with 1704 DSP processing units. The internal resources of the XCVM2152 are shown below:

	VM1102	VM1302	VM1402	VM1502	VM1802	VM2152	VM2202	VM2302	VM2502	VM2902
Programmable Logic	System Logic Cells (K)	329	703	1,238	981	1,968	757	1,139	1,575	1,969
	LUTs	150,272	321,536	565,760	448,512	899,840	346,112	520,704	719,872	900,224
	DSP Engines	464	848	1,696	1,312	1,968	1,704	1,312	1,904	3,984
	NoC Master / NoC Slave Ports	5	9	18	21	28	12	21	30	28
	Distributed RAM (Mb)	5	10	17	14	27	11	16	22	27
Memory	Total Block RAM (Mb)	5	18	40	34	34	27	21	49	47
	Total UltraRAM (Mb)	44	50	80	130	130	54	74	127	190
	Total PL Memory (Mb)	54	78	137	178	191	92	111	198	264
	DDR4 Memory Controllers	1	2	4	3	4	-	3	3	4
	DDR5 Memory Controllers	-	-	-	-	-	4	-	-	-
Processing System	DDR Bus Widths	64	128	256	192	256	128	192	192	256
	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC								
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM w/ECC								
	Memory	256 KB On-Chip Memory w/ECC								
	Connectivity	Ethernet (x2); USB 2.0 (x1); UART (x2); SPI (x2); I2C (x2); CAN-FD (x2)								
Serial Transceivers	GTy Transceivers	0	24	24	44	44	0	0	0	0
	GTYP Transceivers	8	0	0	0	0	8	32 ⁽¹⁾	8	16 ⁽¹⁾
	GTM Transceivers (58G ² (112G))	0	0	0	0	0	8 (4)	0	36 (0)	0
Integrated Protocol IP	PCIe® w/DMA (CPM4)	-	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	-	-	-	-
	PCIe w/DMA (CPM5)	-	-	-	-	-	2 x Gen5x8	-	2 x Gen5x8	-
	PCIe (PL PCIe4)	-	2 x Gen4x8	2 x Gen4x8	4 x Gen4x8	4 x Gen4x8	-	-	-	-
	PCIe (PL PCIe5)	1 x Gen4x8	-	-	-	-	2 x Gen5x4	4 x Gen5x4	2 x Gen5x4	-
	100G Multirate Ethernet MAC	1	2	2	4	4	2	2	6	6
Ordering Information	600G Ethernet MAC	-	-	-	-	-	1	-	-	-
	400G High Speed Crypto	-	-	-	-	-	1	-	-	-
	Extended Temp ³	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE					-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE, -3HSE	-1MSE, -1MLU, -1LSI, -1LLI, -2MSI, -2MLI, -2HSE
	Industrial Temp ³	-1MSI, -1MLU, -1LSI, -1LLI, -2MSI, -2MLI, -2LLI, -2HSE					-1MSI, -1MLU, -1LSI, -1LLI, -2MSI, -2MLI, -2HSE	-1MSI, -1MLU, -1LSI, -1LLI, -2MSI, -2MLI, -2HSE	-1MSI, -1MLU, -1LSI, -1LLI, -2MSI, -2MLI	-1MSI, -1MLU, -1LSI, -1LLI, -2MSI, -2MLI

Figure 2.2.2 - Internal resources of VM2152

2.3 Clock

The ACVM2152 SoM provides a reference clock and an RTC real-time clock for the PS system and PL logic section, respectively , allowing the PS system and PL logic to operate independently. A schematic diagram of the clock circuit design is shown in Figure 2.3.1 below :

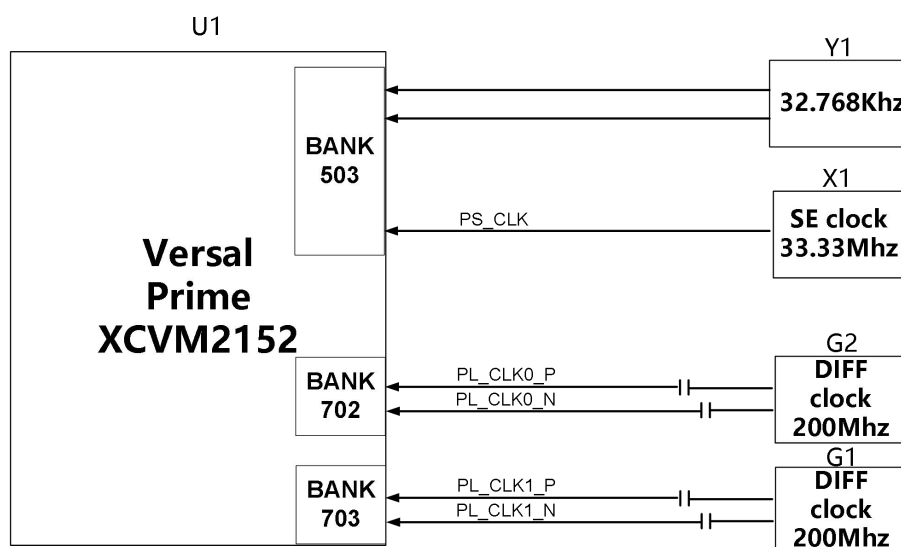


Figure 2.3.1 - SoM clock source

PS system RTC real-time clock

The passive crystal Y1 on the SoM provides a 32.768kHz real-time clock source for the PS system . The crystal is connected to the RTC_PADI_503 and RTC_PADI_503 pins of the VE2302 chip .

PS system clock source

X1 crystal oscillator on the SoM provides a 33.333MHz clock input for the PS system . The clock

input is connected to the PS_REF_CLK_503 pin of the BANK503 of the VE2302 chip .

PL system clock source

The SoM provides two differential 100 MHz PL system clock sources for the LPDDR5 controller's reference clock. The crystal oscillator output is connected to the Global Clock (GC) of PL BANK702 and PL BANK703, which powers the DDR4 controller and user logic circuits within the FPGA..

PL clock pin assignment:

Signal name	VM2152 pin name	VM2152 pin number
PL_CLK0_N	IO_L3N_GC_H00P7_M0P71_702	AT12
PL_CLK0_P	IO_L3P_GC_H00P6_M0P70_702	AR13
PL_CLK 1_N	IO_L19N_GC_H10P7_M1P103_703	AH18
PL_CLK 1_P	IO_L19P_GC_H10P6_M1P102_703	AG19

Table 2.3.1 - PL Clock Pin Assignment

2.4 LPDDR5 DRAM

The ACVM2152 SoM is equipped with two Micron 2GB LPDDR5 chips , model MT62F512M32D1DS-023AIT:E. These two LPDDR5 chips are connected to the X5 I / O ports of BANK700 , 701, 702 , 703 , 704 , and 705 , forming a 64-bit data bus bandwidth and a capacity of 2GB. The maximum operating data rate of the LP DDR5 SDRAM can reach 8533 Mbps . The specific configuration of the LPDDR5 SDRAM is shown in Table 2.4.1 below .

Position	Chip Model	Capacity	Factory
U 2, U3	MT62F512M32D1DS-023 AIT:E	512 M x 32 bit	Micron

Table 2.4.1 - LP DDR 5 SDRAM Configuration

LPDDR5 requires strict consideration of signal integrity. During circuit and PCB design, we have fully considered matching resistors/terminating resistors, trace impedance control, and trace length equalization to ensure the high -speed and stable operation of LPDDR5 . The hardware connection method of LPDDR5 is shown in Figure 2.4.1 :

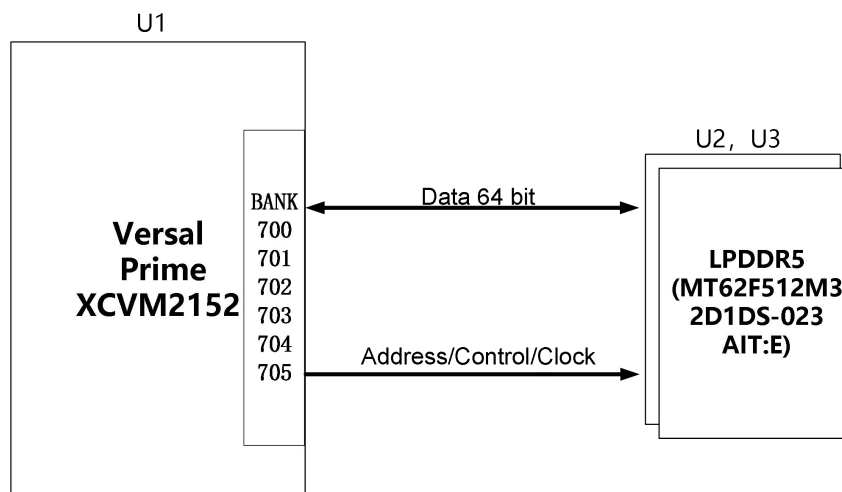


Figure 2.4.1 - Partial schematic of LP DDR 5 DRAM

LPDDR5 SDRAM pin assignment:

Signal name	pin name	pin number
LPDDR5_CH0_DMI0_A	IO_L11P_H0O2P6_M0P22_700	AM2
LPDDR5_CH0_DQS0_N_A	IO_L13N_XCC_H0O3P3_M0P27_700	AM5
LPDDR5_CH0_DQS0_P_A	IO_L13P_XCC_H0O3P2_M0P26_700	AL5
LPDDR5_CH0_DQ0_A	IO_L14N_H0O3P5_M0P29_700	AM7
LPDDR5_CH0_DQ1_A	IO_L8P_H0O2P0_M0P16_700	AN6
LPDDR5_CH0_DQ2_A	IO_L14P_H0O3P4_M0P28_700	AL6
LPDDR5_CH0_DQ3_A	IO_L8N_H0O2P1_M0P17_700	AP5
LPDDR5_CH0_DQ4_A	IO_L12P_H0O3P0_M0P24_700	AL3
LPDDR5_CH0_DQ5_A	IO_L12N_H0O3P1_M0P25_700	AM4
LPDDR5_CH0_DQ6_A	IO_L10N_H0O2P5_M0P21_700	AP2
LPDDR5_CH0_DQ7_A	IO_L10P_H0O2P4_M0P20_700	AN3
LPDDR5_CH0_WCK0_C_A	IO_L9N_XCC_H0O2P3_M0P19_700	AP3
LPDDR5_CH0_WCK0_T_A	IO_L9P_XCC_H0O2P2_M0P18_700	AN4
LPDDR5_CH0_DMI1_A	IO_L3P_GC_H0O0P6_M0P6_700	AR2
LPDDR5_CH0_DQS1_N_A	IO_L5N_XCC_H0O1P3_M0P11_700	AT6
LPDDR5_CH0_DQS1_P_A	IO_L5P_XCC_H0O1P2_M0P10_700	AR5
LPDDR5_CH0_DQ8_A	IO_L2N_H0O0P5_M0P5_700	AT1

Signal name	pin name	pin number
LPDDR5_CH0_DQ9_A	IO_L4P_H0O1P0_M0P8_700	AR4
LPDDR5_CH0_DQ10_A	IO_L4N_H0O1P1_M0P9_700	AT4
LPDDR5_CH0_DQ11_A	IO_L2P_H0O0P4_M0P4_700	AR1
LPDDR5_CH0_DQ12_A	IO_L6N_H0O1P5_M0P13_700	AT7
LPDDR5_CH0_DQ13_A	IO_L6P_H0O1P4_M0P12_700	AR7
LPDDR5_CH0_DQ14_A	IO_L0N_H0O0P1_M0P1_700	AU6
LPDDR5_CH0_DQ15_A	IO_L0P_H0O0P0_M0P0_700	AU5
LPDDR5_CH0_WCK1_C_A	IO_L1N_XCC_H0O0P3_M0P3_700	AU3
LPDDR5_CH0_WCK1_T_A	IO_L1P_XCC_H0O0P2_M0P2_700	AU2
LPDDR5_CH0_CK_N	IO_L31N_H1O3P7_M0P63_701	AU9
LPDDR5_CH0_CK_P	IO_L31P_H1O3P6_M0P62_701	AU8
LPDDR5_CH0_CS0_A	IO_L19P_GC_H1O0P6_M0P38_701	AH8
LPDDR5_CH0_CS1_A	IO_L2P_H0O0P4_M0P68_702	AU11
LPDDR5_CH0_CA0	IO_L11N_H0O2P7_M0P23_700	AN1
LPDDR5_CH0_CA1	IO_L3N_GC_H0O0P7_M0P7_700	AT3
LPDDR5_CH0_CA2	IO_L15P_H0O3P6_M0P30_700	AK6
LPDDR5_CH0_CA3	IO_L7P_H0O1P6_M0P14_700	AN7
LPDDR5_CH0_CA4	IO_L15N_H0O3P7_M0P31_700	AK7
LPDDR5_CH0_CA5	IO_L27N_H1O2P7_M0P55_701	AP9
LPDDR5_CH0_CA6	IO_L7N_H0O1P7_M0P15_700	AP6
LPDDR5_CH0_DMI0_B	IO_L23P_H1O1P6_M0P46_701	AL11
LPDDR5_CH0_DQS0_N_B	IO_L17N_XCC_H1O0P3_M0P35_701	AG10
LPDDR5_CH0_DQS0_P_B	IO_L17P_XCC_H1O0P2_M0P34_701	AF10
LPDDR5_CH0_DQ0_B	IO_L16P_H1O0P0_M0P32_701	AE11
LPDDR5_CH0_DQ1_B	IO_L18P_H1O0P4_M0P36_701	AG9
LPDDR5_CH0_DQ2_B	IO_L22N_H1O1P5_M0P45_701	AJ11
LPDDR5_CH0_DQ3_B	IO_L22P_H1O1P4_M0P44_701	AH11

Signal name	pin name	pin number
LPDDR5_CH0_DQ4_B	IO_L16N_H1O0P1_M0P33_701	AF11
LPDDR5_CH0_DQ5_B	IO_L20P_H1O1P0_M0P40_701	AJ8
LPDDR5_CH0_DQ6_B	IO_L20N_H1O1P1_M0P41_701	AK9
LPDDR5_CH0_DQ7_B	IO_L18N_H1O0P5_M0P37_701	AH9
LPDDR5_CH0_WCK0_C_B	IO_L21N_XCC_H1O1P3_M0P43_701	AK10
LPDDR5_CH0_WCK0_T_B	IO_L21P_XCC_H1O1P2_M0P42_701	AJ10
LPDDR5_CH0_DMI1_B	IO_L27P_H1O2P6_M0P54_701	AN9
LPDDR5_CH0_DQS1_N_B	IO_L25N_XCC_H1O2P3_M0P51_701	AM8
LPDDR5_CH0_DQS1_P_B	IO_L25P_XCC_H1O2P2_M0P50_701	AL8
LPDDR5_CH0_DQ8_B	IO_L24P_H1O2P0_M0P48_701	AL9
LPDDR5_CH0_DQ9_B	IO_L26P_H1O2P4_M0P52_701	AP8
LPDDR5_CH0_DQ10_B	IO_L24N_H1O2P1_M0P49_701	AM10
LPDDR5_CH0_DQ11_B	IO_L28P_H1O3P0_M0P56_701	AN10
LPDDR5_CH0_DQ12_B	IO_L28N_H1O3P1_M0P57_701	AP11
LPDDR5_CH0_DQ13_B	IO_L30P_H1O3P4_M0P60_701	AR10
LPDDR5_CH0_DQ14_B	IO_L30N_H1O3P5_M0P61_701	AT9
LPDDR5_CH0_DQ15_B	IO_L26N_H1O2P5_M0P53_701	AR8
LPDDR5_CH0_WCK1_C_B	IO_L29N_XCC_H1O3P3_M0P59_701	AT10
LPDDR5_CH0_WCK1_T_B	IO_L29P_XCC_H1O3P2_M0P58_701	AR11
LPDDR5_CH0_CK_N	IO_L31N_H1O3P7_M0P63_701	AU9
LPDDR5_CH0_CK_P	IO_L31P_H1O3P6_M0P62_701	AU8
LPDDR5_CH0_CA0	IO_L11N_H0O2P7_M0P23_700	AN1
LPDDR5_CH0_CA1	IO_L3N_GC_H0O0P7_M0P7_700	AT3
LPDDR5_CH0_CA2	IO_L15P_H0O3P6_M0P30_700	AK6
LPDDR5_CH0_CA3	IO_L7P_H0O1P6_M0P14_700	AN7
LPDDR5_CH0_CA4	IO_L15N_H0O3P7_M0P31_700	AK7
LPDDR5_CH0_CA5	IO_L27N_H1O2P7_M0P55_701	AP9

Signal name	pin name	pin number
LPDDR5_CH0_CA6	IO_L7N_H001P7_M0P15_700	AP6
LPDDR5_CH0_CS0_B	IO_L19N_GC_H1O0P7_M0P39_701	AJ7
LPDDR5_CH0_CS1_B	IO_L2N_H000P5_M0P69_702	AU12
LPDDR5_CH0_RESET	IO_L23N_H1O1P7_M0P47_701	AM11
LPDDR5_CH1_DMI0_A	IO_L19P_GC_H1O0P6_M1P166_705	AG27
LPDDR5_CH1_DQS0_N_A	IO_L21N_XCC_H1O1P3_M1P171_705	AL27
LPDDR5_CH1_DQS0_P_A	IO_L21P_XCC_H1O1P2_M1P170_705	AK27
LPDDR5_CH1_DQ0_A	IO_L20P_H1O1P0_M1P168_705	AJ28
LPDDR5_CH1_DQ1_A	IO_L20N_H1O1P1_M1P169_705	AK28
LPDDR5_CH1_DQ2_A	IO_L22P_H1O1P4_M1P172_705	AL26
LPDDR5_CH1_DQ3_A	IO_L16P_H1O0P0_M1P160_705	AE26
LPDDR5_CH1_DQ4_A	IO_L16N_H1O0P1_M1P161_705	AE27
LPDDR5_CH1_DQ5_A	IO_L22N_H1O1P5_M1P173_705	AM26
LPDDR5_CH1_DQ6_A	IO_L18P_H1O0P4_M1P164_705	AF26
LPDDR5_CH1_DQ7_A	IO_L18N_H1O0P5_M1P165_705	AG25
LPDDR5_CH1_WCK0_C_A	IO_L17N_XCC_H1O0P3_M1P163_705	AG24
LPDDR5_CH1_WCK0_T_A	IO_L17P_XCC_H1O0P2_M1P162_705	AF25
LPDDR5_CH1_DMI1_A	IO_L27P_H1O2P6_M1P182_705	AP26
LPDDR5_CH1_DQS1_N_A	IO_L29N_XCC_H1O3P3_M1P187_705	AT27
LPDDR5_CH1_DQS1_P_A	IO_L29P_XCC_H1O3P2_M1P186_705	AR26
LPDDR5_CH1_DQ8_A	IO_L24P_H1O2P0_M1P176_705	AL29
LPDDR5_CH1_DQ9_A	IO_L24N_H1O2P1_M1P177_705	AM29
LPDDR5_CH1_DQ10_A	IO_L26P_H1O2P4_M1P180_705	AN27
LPDDR5_CH1_DQ11_A	IO_L30N_H1O3P5_M1P189_705	AU24
LPDDR5_CH1_DQ12_A	IO_L28P_H1O3P0_M1P184_705	AR28
LPDDR5_CH1_DQ13_A	IO_L28N_H1O3P1_M1P185_705	AT28
LPDDR5_CH1_DQ14_A	IO_L26N_H1O2P5_M1P181_705	AP27

Signal name	pin name	pin number
LPDDR5_CH1_DQ15_A	IO_L30P_H1O3P4_M1P188_705	AT25
LPDDR5_CH1_WCK1_C_A	IO_L25N_XCC_H1O2P3_M1P179_705	AN28
LPDDR5_CH1_WCK1_T_A	IO_L25P_XCC_H1O2P2_M1P178_705	AM28
LPDDR5_CH1_DMI0_B	IO_L7P_H0O1P6_M1P142_704	AL23
LPDDR5_CH1_DQS0_N_B	IO_L1N_XCC_H0O0P3_M1P131_704	AU21
LPDDR5_CH1_DQS0_P_B	IO_L1P_XCC_H0O0P2_M1P130_704	AT21
LPDDR5_CH1_DQ0_B	IO_L6P_H0O1P4_M1P140_704	AM22
LPDDR5_CH1_DQ1_B	IO_L4P_H0O1P0_M1P136_704	AN24
LPDDR5_CH1_DQ2_B	IO_L4N_H0O1P1_M1P137_704	AP24
LPDDR5_CH1_DQ3_B	IO_L6N_H0O1P5_M1P141_704	AN22
LPDDR5_CH1_DQ4_B	IO_L2P_H0O0P4_M1P132_704	AR22
LPDDR5_CH1_DQ5_B	IO_L2N_H0O0P5_M1P133_704	AT22
LPDDR5_CH1_DQ6_B	IO_L0N_H0O0P1_M1P129_704	AU23
LPDDR5_CH1_DQ7_B	IO_L0P_H0O0P0_M1P128_704	AT24
LPDDR5_CH1_WCK0_C_B	IO_L5N_XCC_H0O1P3_M1P139_704	AP21
LPDDR5_CH1_WCK0_T_B	IO_L5P_XCC_H0O1P2_M1P138_704	AN21
LPDDR5_CH1_DMI1_B	IO_L11P_H0O2P6_M1P150_704	AG21
LPDDR5_CH1_DQS1_N_B	IO_L9N_XCC_H0O2P3_M1P147_704	AJ23
LPDDR5_CH1_DQS1_P_B	IO_L9P_XCC_H0O2P2_M1P146_704	AH24
LPDDR5_CH1_DQ8_B	IO_L12N_H0O3P1_M1P153_704	AH23
LPDDR5_CH1_DQ9_B	IO_L8N_H0O2P1_M1P145_704	AM20
LPDDR5_CH1_DQ10_B	IO_L12P_H0O3P0_M1P152_704	AG22
LPDDR5_CH1_DQ11_B	IO_L8P_H0O2P0_M1P144_704	AL20
LPDDR5_CH1_DQ12_B	IO_L10P_H0O2P4_M1P148_704	AH20
LPDDR5_CH1_DQ13_B	IO_L14N_H0O3P5_M1P157_704	AF20
LPDDR5_CH1_DQ14_B	IO_L14P_H0O3P4_M1P156_704	AE21
LPDDR5_CH1_DQ15_B	IO_L10N_H0O2P5_M1P149_704	AJ20

Signal name	pin name	pin number
LPDDR5_CH1_WCK1_C_B	IO_L13N_XCC_H003P3_M1P155_704	AF23
LPDDR5_CH1_WCK1_T_B	IO_L13P_XCC_H003P2_M1P154_704	AF22
LPDDR5_CH1_CK_N	IO_L15N_H003P7_M1P159_704	AE24
LPDDR5_CH1_CK_P	IO_L15P_H003P6_M1P158_704	AE23
LPDDR5_CH1_CS0_B	IO_L3N_GC_H000P7_M1P135_704	AR23
LPDDR5_CH1_CS1_B	IO_L18N_H100P5_M1P101_703	AG18
LPDDR5_CH1_CS0_A	IO_L3P_GC_H000P6_M1P134_704	AP23
LPDDR5_CH1_CS1_A	IO_L18P_H100P4_M1P100_703	AF17
LPDDR5_CH1_CA0	IO_L11N_H002P7_M1P151_704	AH21
LPDDR5_CH1_CA1	IO_L23P_H101P6_M1P174_705	AM25
LPDDR5_CH1_CA2	IO_L23N_H101P7_M1P175_705	AN25
LPDDR5_CH1_CA3	IO_L31N_H103P7_M1P191_705	AU27
LPDDR5_CH1_CA4	IO_L27N_H102P7_M1P183_705	AR25
LPDDR5_CH1_CA5	IO_L19N_GC_H100P7_M1P167_705	AH27
LPDDR5_CH1_CA6	IO_L31P_H103P6_M1P190_705	AU26
LPDDR5_CH1_RESET	IO_L7N_H001P7_M1P143_704	AM23

Table 2.4.2 - LPDDR5 SDRAM Pin Assignments

2.5 QSPI Flash

The ACVM2152 SoM is equipped with two 512Gbit Quad-SPI FLASH chips, model MT25QU512ABA1EW9-0SIT, which use the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can store the FPGA configuration binary file and other user data files. Specific models and related parameters of the QSPI FLASH are shown in Table 2.5.1 .

Position	Chip type	Capacity	Factory
U5, U9	MT25QU512ABA1EW9-0SIT	512Gbit	Micron

Table 2.5.1 - QSPI Flash Models and Parameters

The QSPI FLASH is connected to the pins of BANK 500 of the FPGA chip, with the clock pin connected to PMC_MIO of BANK 500. Figure 2.5.1 shows a schematic diagram of the connection between the QSPI Flash and the FPGA chip.

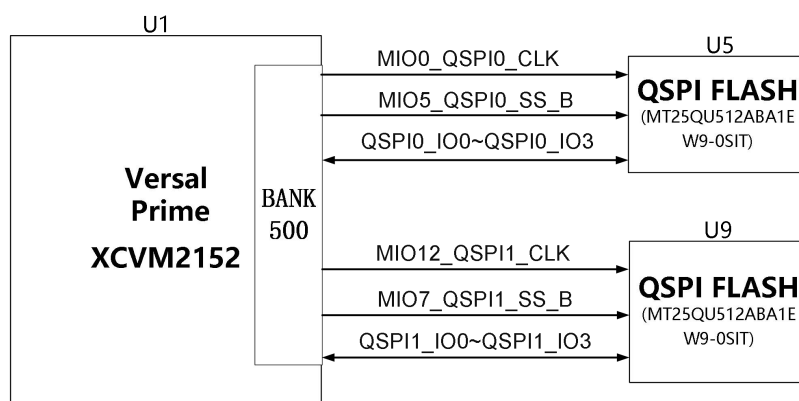


Figure 2.5.1 - QSPI Flash Connection Diagram

Chip pin assignment:

Signal name	FPGA pin names	FPGA pin numbers
MIO0_QSPI 0 _S CLK	PMC_MIO0_500	W7
MIO5_QSPI 0 _S S_B	PMC_MIO5_500	R6
MIO4_QSPI 0 _IO 0	PMC_MIO4_500	T6
MIO1_QSPI 0 _IO 1	PMC_MIO1_500	W6
MIO2_QSPI 0 _IO 2	PMC_MIO2_500	V6
MIO3_QSPI 0 _IO 3	PMC_MIO3_500	U6
MIO12_QSPI 1 _CLK	PMC_MIO12_500	U4
MIO7_QSPI 1 _SS_B	PMC_MIO7_500	T5
MIO8_QSPI 1 _IO 0	PMC_MIO8_500	U5
MIO9_QSPI 1 _IO 1	PMC_MIO9_500	V5
MIO10_QSPI 1 _IO 2	PMC_MIO10_500	W4
MIO11_QSPI 1 _IO 3	PMC_MIO11_500	V4

Table 2.5.2 - QSPI Flash Pin Assignment

2.6 eMMC Flash

The ACVM2152 SoM is equipped with a large-capacity 32GB eMMC FLASH chip, model MTFC32GAPALBH-IT from Micron . It supports the JEDEC e-MMC V5.1 standard HS-MMC interface (compatible with V5.0), and supports voltage levels of 1.8V or 3.3V. The data width between the eMMC FLASH and the FPGA is 8 bits. Due to the large capacity and non-volatile nature of the eMMC FLASH, it can be used as a large-capacity storage device in FPGA systems, such as storing ARM application programs, system files, and other user data files. Specific models and related parameters of the eMMC FLASH are shown in Table 2.6.1 .

Position	Chip type	Capacity	Factory
U28	MTFC32GAPALBH-IT	32 GB	Micron

Table 2.6.1 - eMMC Flash Models and Parameters

The eMMC FLASH is connected to the IO port of BANK501 on the FPGA chip. During system design, the GPIO functions of these ports must be configured as eMMC interfaces. Figure 2.6.1 shows a schematic representation of the eMMC Flash in the circuit diagram..

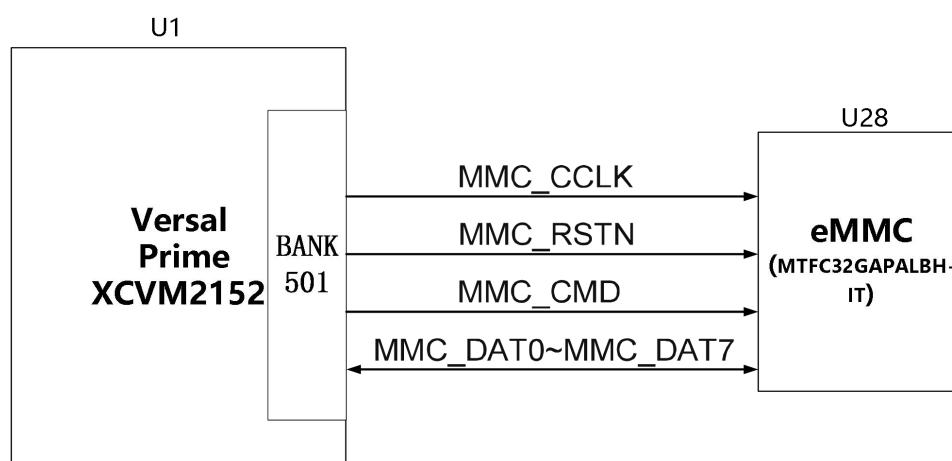


Figure 2.6.1 - Schematic diagram of eMMC Flash connection

eMMC configuration chip pin assignment:

Signal name	FPGA pin names	FPGA pin numbers	Remark
MMC_CCLK	PMC_MIO38_501	Y5	eMMC clock signal
MMC_RSTN	PMC_MIO49_501	AA1	eMMC reset signal (active low)
MMC_CMD	PMC_MIO40_501	AB4	eMMC Commands/Response Signals
MMC_DAT0	PMC_MIO41_501	AC4	eMMC Data Channel 0
MMC_DAT1	PMC_MIO42_501	AB3	eMMC Data Channel 1
MMC_DAT2	PMC_MIO43_501	AA3	eMMC Data Channel 2
MMC_DAT3	PMC_MIO44_501	Y3	eMMC Data Channel 3
MMC_DAT4	PMC_MIO45_501	W2	eMMC Data Channel 4
MMC_DAT5	PMC_MIO46_501	AA2	eMMC Data Channel 5
MMC_DAT6	PMC_MIO47_501	AB2	eMMC Data Channel 6
MMC_DAT7	PMC_MIO48_501	AC2	eMMC Data Channel 7

Table 2.6.2 - eMMC Pin Assignments

2.7 Power Supply

The ACVM2152 SoM is powered by +12V, and is powered by the carrier board. The SoM uses a MAX20796GFB+ power supply chip to output 60A of current to provide 0.8V core power to the XCVM2152. Power is supplied to the BANK500, 501, 502, 400, 401, 700, 705, 706, 707, 708, 709, 710, 711, and the transceiver via a DC-DC power supply.

Because the Versal Prime FPGA has specific power-on sequence requirements, the power-on sequence has been designed according to the chip's power requirements in the circuit design as follows:

The power-on requirements for the PMC power supply section are: PMC_VCCO (1.8V) -> VCC_PMC (0.8V) -> VCCAUX_PMC (1.5V).

The power-on requirements for the LPD power supply section are: VCCAUX_PMC (1.5V) -> LPD_VCCO_502 (1.8V) -> VCC_PSLP (0.8V).

The power-on requirements for the FPD power supply section are: VCC_PSFP(0.8V) -> VCAUX_PMC(1.5V) -> VCC_PSFP(0.8V).

The power-on requirements for the SPD (SYSTEM) power supply section are: VCCAUX_PMC (1.5V) -> VCCO_700 (1.0V) -> VCC_SOC/VCC_IO (0.8V) -> VCCAUX (1.5V).

The power-on requirements for the PL power supply are: VCCAUX -> PL_VCCO_HD (PL_VCCO_HP) -> VCCINT -> VCC_RAM (VCCINT_GT) -> GTM_AVCC (GTYP_AVCC) -> GTM_AVTT (GTYP_AVTT)

The design block diagram is shown in Figure 2.7.1;

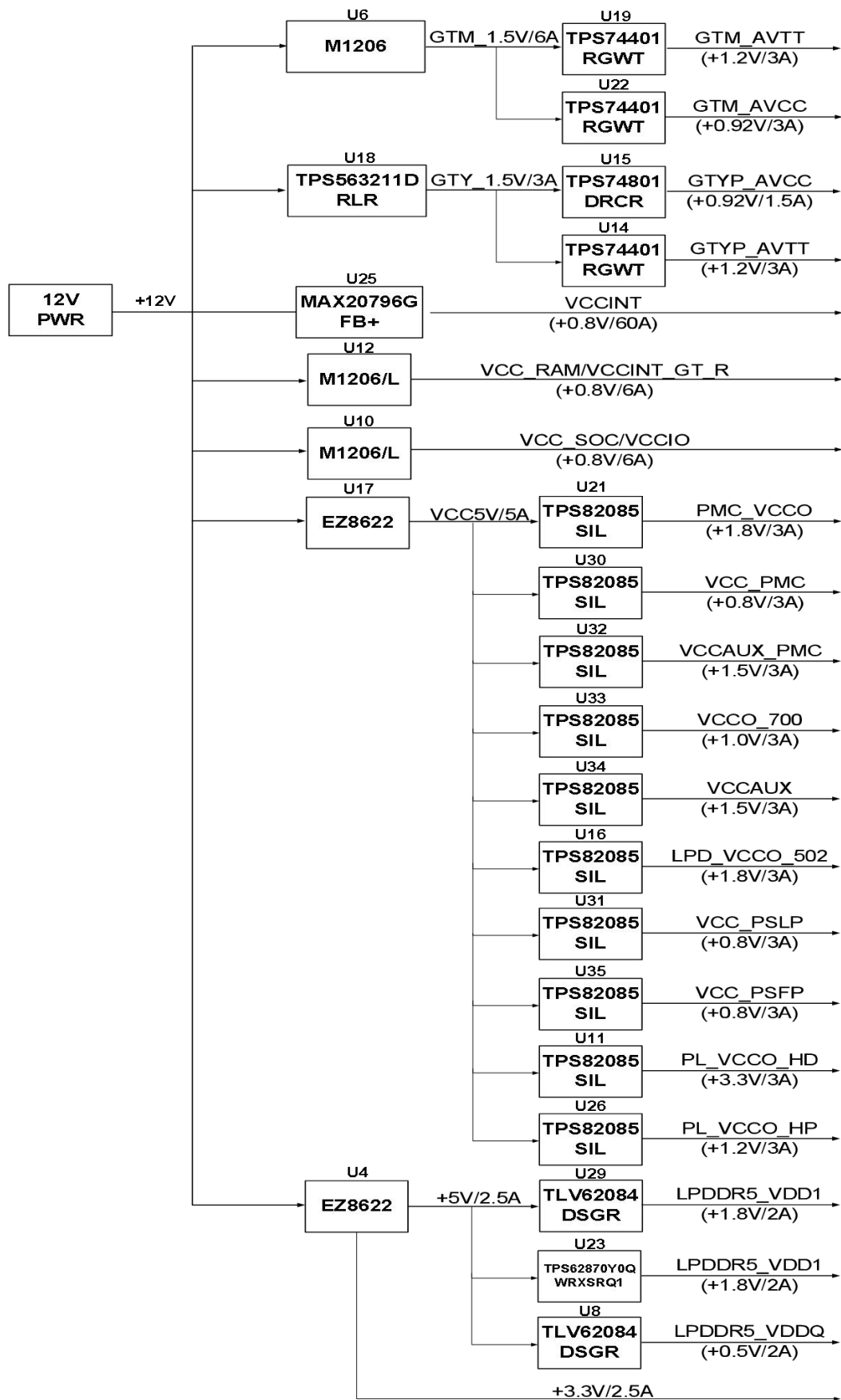


Figure 2.7.1- Power supply design block diagram

2.8 Expansion Interface

The backside of the SoM features three high-speed expansion ports, connected to the base plate via three 240-pin inter-board connectors (Samtec: ADF6-60-03.5-L-4-2-A-T). The FPGA's IO pins are linked to these ports via differential routing. The connector pins have a pitch of 0.5 mm, and their mating with the base plate's female connector enables high-speed data communication.

Expansion port J5

240 -pin connector J5 is used to connect the VCCIN power supply (+12V) and ground of the carrier board, the general-purpose PS I/O pins of the FPGA, and the high-speed transceiver . The pin assignments for the J5_AB expansion port are shown in Table 2.8.1 .

J5 pin	Signal name	FPGA pin numbers	Level Standard	J5 pin	Signal name	FPGA pin numbers	Level Standard
A1	GND	-	GND	B1	GND	-	GND
A2	GND	-	GND	B2	GND	-	GND
A3	103_TX3_N	B6	1.2V	B3	103_TX3_P	B7	1.2V
A4	GND	-	GND	B4	GND	-	GND
A5	GND	-	GND	B5	GND	-	GND
A6	103_TX2_N	D6	1.2V	B6	103_TX2_P	D7	1.2V
A7	GND	-	GND	B7	GND	-	GND
A8	GND	-	GND	B8	GND	-	GND
A9	103_TX1_N	E4	1.2V	B9	103_TX1_P	E5	1.2V
A10	GND	-	GND	B10	GND	-	GND
A11	GND	-	GND	B11	GND	-	GND
A12	103_TX0_N	F6	1.2V	B12	103_TX0_P	F7	1.2V
A13	GND	-	GND	B13	GND	-	GND
A14	GND	-	GND	B14	GND	-	GND
A15	103_CLK1_N	H6	1.2V	B15	103_CLK1_P	H7	1.2V
A16	GND	-	GND	B16	GND	-	GND
A17	GND	-	GND	B17	GND	-	GND
A18	102_TX3_N	G4	1.2V	B18	102_TX3_P	G5	1.2V
A19	GND	-	GND	B19	GND	-	GND

J5 pin	Signal name	FPGA pin numbers	Level Standard	J5 pin	Signal name	FPGA pin numbers	Level Standard
A20	GND	-	GND	B20	GND	-	GND
A21	102_TX2_N	J4	1.2V	B21	102_TX2_P	J5	1.2V
A22	GND	-	GND	B22	GND	-	GND
A23	GND	-	GND	B23	GND	-	GND
A24	102_TX1_N	L4	1.2V	B24	102_TX1_P	L5	1.2V
A25	GND	-	GND	B25	GND	-	GND
A26	GND	-	GND	B26	GND	-	GND
A27	102_TX0_N	N4	1.2V	B27	102_TX0_P	N5	1.2V
A28	GND	-	GND	B28	GND	-	GND
A29	GND	-	GND	B29	GND	-	GND
A30	102_CLK1_P	M7	1.2V	B30	102_CLK1_N	M6	1.2V
A31	GND	-	GND	B31	GND	-	GND
A32	PS_MIO14	R3	1.8V	B32	PS_MIO21	P2	1.8V
A33	PS_MIO20	T2	1.8V	B33	PS_MIO22	P1	1.8V
A34	GND	-	GND	B34	GND	-	GND
A35	PS_MIO23	R1	1.8V	B35	PS_MIO19	U2	1.8V
A36	PS_MIO51	W1	1.8V	B36	PS_MIO18	V2	1.8V
A37	GND	-	GND	B37	GND	-	GND
A38	PS_MIO15	T3	1.8V	B38	PS_MIO17	W3	1.8V
A39	PS_MIO13	R4	1.8V	B39	PS_MIO29	AC7	1.8V
A40	GND	-	GND	B40	GND	-	GND
A41	LPD_MIO1	AE8	1.8V	B41	PS_MIO35	AC5	1.8V
A42	LPD_MIO0	AD8	1.8V	B42	PS_MIO27	AB8	1.8V
A43	GND	-	GND	B43	GND	-	GND
A44	LPD_MIO7	AE6	1.8V	B44	LPD_MIO19	AD3	1.8V
A45	LPD_MIO13	AF5	1.8V	B45	LPD_MIO11	AH5	1.8V
A46	GND	-	GND	B46	GND	-	GND

J5 pin	Signal name	FPGA pin numbers	Level Standard	J5 pin	Signal name	FPGA pin numbers	Level Standard
A47	LPD_MIO25	AC1	1.8V	B47	LPD_MIO24	AD1	1.8V
A48	LPD_MIO23	AE1	1.8V	B48	LPD_MIO18	AE3	1.8V
A49	GND	-	GND	B49	GND	-	GND
A50	LPD_MIO22	AF1	1.8V	B50	LPD_MIO21	AF2	1.8V
A51	LPD_MIO2	AF8	1.8V	B51	LPD_MIO15	AD4	1.8V
A52	GND	-	GND	B52	GND	-	GND
A53	LPD_MIO16	AE4	1.8V	B53	-	-	-
A54	-	-	-	B54	-	-	-
A55	PW_PG	-	3.3V	B55	VCC_BATT	-	VCC_BATT
A56	PS_POR_B	AA15	3.3V	B56	DONE	AG3	1.8V
A57	GND	-	GND	B57	GND	-	GND
A58	+12V	-	+12V	B58	+12V	-	+12V
A59	+12V	-	+12V	B59	+12V	-	+12V
A60	+12V	-	+12V	B60	+12V	-	+12V

Table 2.8.1 - Pin Assignment for Expansion Port J5_AB

Expansion port J5_CD

The pin assignments for the J5_CD expansion port are shown in Table 2.8.2:

J5 pin	Signal name	FPGA pin numbers	Level Standard	J5 pin	Signal name	FPGA pin numbers	Level Standard
C1	GND	-	GND	D1	GND		GND
C2	103_RX3_N	A3	1.2V	D2	103_RX3_P	A4	GND
C3	GND	-	GND	D3	GND		1.2V
C4	GND	-	GND	D4	GND		GND
C5	103_RX2_N	B1	1.2V	D5	103_RX2_P	B2	GND
C6	GND	-	GND	D6	GND		1.2V
C7	GND	-	GND	D7	GND		GND
C8	103_RX1_N	C3	1.2V	D8	103_RX1_P	C4	GND
C9	GND	-	GND	D9	GND		1.2V

J5 pin	Signal name	FPGA numbers	pin	Level Standard	J5 pin	Signal name	FPGA numbers	pin	Level Standard
C10	GND	-		GND	D10	GND			GND
C11	103_RX0_N	D1		1.2V	D11	103_RX0_P	D2		GND
C12	GND	-		GND	D12	GND			1.2V
C13	GND	-		GND	D13	GND			GND
C14	103_CLK0_N	K6		1.2V	D14	103_CLK0_P	K7		GND
C15	GND	-		GND	D15	GND			1.2V
C16	GND	-		GND	D16	GND			GND
C17	102_RX3_N	F1		1.2V	D17	102_RX3_P	F2		GND
C18	GND	-		GND	D18	GND			1.2V
C19	GND	-		GND	D19	GND			GND
C20	102_RX2_N	H1		1.2V	D20	102_RX2_P	H2		GND
C21	GND	-		GND	D21	GND			1.2V
C22	GND	-		GND	D22	GND			GND
C23	102_RX1_N	K1		1.2V	D23	102_RX1_P	K2		GND
C24	GND	-		GND	D24	GND			1.2V
C25	GND	-		GND	D25	GND			GND
C26	102_RX0_N	M1		1.2V	D26	102_RX0_P	M2		GND
C27	GND	-		GND	D27	GND			1.2V
C28	GND	-		GND	D28	GND			GND
C29	102_CLK0_N	N8		1.2V	D29	102_CLK0_P	N9		GND
C30	GND	-		GND	D30	GND	-		GND
C31	GND	-		GND	D31	GND	-		GND
C32	PS_MIO30	AB7		1.8V	D32	PS_MIO31	AA7		1.8V
C33	PS_MIO24	T1		1.8V	D33	PS_MIO33	AA6		1.8V
C34	GND	-		GND	D34	GND	-		GND
C35	PS_MIO25	V1		1.8V	D35	PS_MIO32	Y6		1.8V
C36	PS_MIO16	U3		1.8V	D36	PS_MIO34	AC6		1.8V

J5 pin	Signal name	FPGA numbers	pin	Level Standard	J5 pin	Signal name	FPGA numbers	pin	Level Standard
C37	GND	-		GND	D37	GND	-		GND
C38	PS_MIO26	AA8		1.8V	D38	PS_MIO50	Y1		1.8V
C39	PS_MIO37	AA5		1.8V	D39	PS_MIO36	AB5		1.8V
C40	GND	-		GND	D40	GND	-		GND
C41	LPD_MIO5	AD7		1.8V	D41	PS_MIO28	AC8		1.8V
C42	LPD_MIO6	AD6		1.8V	D42	LPD_MIO8	AF6		1.8V
C43	GND	-		GND	D43	GND	-		GND
C44	LPD_MIO14	AE5		1.8V	D44	LPD_MIO12	AG5		1.8V
C45	LPD_MIO20	AD2		1.8V	D45	LPD_MIO9	AH6		1.8V
C46	GND	-		GND	D46	GND	-		GND
C47	LPD_MIO3	AG7		1.8V	D47	LPD_MIO10	AJ5		1.8V
C48	LPD_MIO4	AF7		1.8V	D48	LPD_MIO17	AF3		1.8V
C49	GND	-		GND	D49	GND	-		GND
C50	PS_MODE3	AJ3		1.8V	D50	PS_MODE1	AH2		1.8V
C51	PS_MODE2	AJ2		1.8V	D51	PS_MODE0	AG2		1.8V
C52	GND	-		GND	D52	GND	-		GND
C53	FPGA_TDO	AJ1		3.3V	D53	FPGA_TMS	AK4		3.3V
C54	FPGA_TCK	AJ4		3.3V	D54	FPGA_TDI	AH1		3.3V
C55	-	-		-	D55	-	-		-
C56	-	-		-	D56	-	-		-
C57	GND	-		GND	D57	GND	-		GND
C58	+12V	-		+12V	D58	+12V	-		+12V
C59	+12V	-		+12V	D59	+12V	-		+12V
C60	+12V	-		+12V	D60	+12V	-		+12V

Table 2.8.2 - Expansion Port J5 _ CD Pin Assignment

Expansion port J6

240 -pin connector J6 is used to connect the PL-side HD IO and HP IO of the FPGA on the carrier board , as well as the high-speed transceiver . The pin assignment of the J6_AB expansion

port is shown in Table 2.8.3 .

J6 pin	Signal name	FPGA numbers	pin	Level Standard	J6 pin	Signal name	FPGA numbers	pin	Level Standard
A1	104_CLK0_P	J9		1.2V	B1	104_CLK0_N	H9		1.2V
A2	GND	-		GND	B2	GND	-		GND
A3	GND	-		GND	B3	GND	-		GND
A4	104_RX0_P	C9		1.2V	B4	104_RX0_N	B9		1.2V
A5	GND	-		GND	B5	GND	-		GND
A6	GND	-		GND	B6	GND	-		GND
A7	104_RX1_P	C11		1.2V	B7	104_RX1_N	B11		1.2V
A8	GND	-		GND	B8	GND	-		GND
A9	GND	-		GND	B9	GND	-		GND
A10	104_RX2_P	C13		1.2V	B10	104_RX2_N	B13		1.2V
A11	GND	-		GND	B11	GND	-		GND
A12	GND	-		GND	B12	GND	-		GND
A13	104_RX3_P	C15		1.2V	B13	104_RX3_N	B15		1.2V
A14	GND	-		GND	B14	GND	-		GND
A15	GND	-		GND	B15	GND	-		GND
A16	105_CLK0_P	J15		1.2V	B16	105_CLK0_N	H15		1.2V
A17	GND	-		GND	B17	GND	-		GND
A18	GND	-		GND	B18	GND	-		GND
A19	105_RX0_P	C17		1.2V	B19	105_RX0_N	B17		1.2V
A20	GND	-		GND	B20	GND	-		GND
A21	GND	-		GND	B21	GND	-		GND
A22	105_RX1_P	C19		1.2V	B22	105_RX1_N	B19		1.2V
A23	GND	-		GND	B23	GND	-		GND
A24	GND	-		GND	B24	GND	-		GND
A25	105_RX2_P	C21		1.2V	B25	105_RX2_N	B21		1.2V
A26	GND	-		GND	B26	GND	-		GND

J6 pin	Signal name	FPGA numbers	pin	Level Standard	J6 pin	Signal name	FPGA numbers	pin	Level Standard
A27	GND	-		GND	B27	GND	-		GND
A28	105_RX3_P	C23		1.2V	B28	105_RX3_N	B23		1.2V
A29	GND	-		GND	B29	GND	-		GND
A30	GND	-		GND	B30	GND	-		GND
A31	B400_L10_N	E28		3.3V	B31	B400_L1_N	E36		3.3V
A32	B400_L10_P	F28		3.3V	B32	B400_L1_P	F35		3.3V
A33	GND	-		GND	B33	GND	-		GND
A34	B400_L6_N	E31		3.3V	B34	B400_L9_N	E29		3.3V
A35	B400_L6_P	F31		3.3V	B35	B400_L9_P	F30		3.3V
A36	GND	-		GND	B36	GND	-		GND
A37	B400_L5_N	F32		3.3V	B37	B400_L7_N	D31		3.3V
A38	B400_L5_P	F33		3.3V	B38	B400_L7_P	E30		3.3V
A39	GND	-		GND	B39	GND	-		GND
A40	B401_L7_N	B32		3.3V	B40	B401_L4_N	A33		3.3V
A41	B401_L7_P	B33		3.3V	B41	B401_L4_P	B34		3.3V
A42	GND	-		GND	B42	GND	-		GND
A43	B401_L10_N	B30		3.3V	B43	B401_L9_N	A30		3.3V
A44	B401_L10_P	C30		3.3V	B44	B401_L9_P	B29		3.3V
A45	GND	-		GND	B45	GND	-		GND
A46	B401_L6_N	C31		3.3V	B46	B401_L8_N	A31		3.3V
A47	B401_L6_P	C32		3.3V	B47	B401_L8_P	A32		3.3V
A48	GND	-		GND	B48	GND	-		GND
A49	B711_L6_N	L32		1.2V	B49	B711_L10_N	J34		1.2V
A50	B711_L6_P	L31		1.2V	B50	B711_L10_P	J33		1.2V
A51	GND	-		GND	B51	GND	-		GND
A52	B711_L11_N	H35		1.2V	B52	B711_L14_N	J36		1.2V
A53	B711_L11_P	H34		1.2V	B53	B711_L14_P	K35		1.2V

J6 pin	Signal name	FPGA numbers	pin	Level Standard	J6 pin	Signal name	FPGA numbers	pin	Level Standard
A54	GND	-		GND	B54	GND	-		GND
A55	B711_L15_N	H37		1.2V	B55	B711_L8_N	M34		1.2V
A56	B711_L15_P	J37		1.2V	B56	B711_L8_P	M33		1.2V
A57	GND	-		GND	B57	GND	-		GND
A58	B711_L13_N	L37		1.2V	B58	B711_L12_N	L35		1.2V
A59	B711_L13_P	K36		1.2V	B59	B711_L12_P	L34		1.2V
A60	-	-		-	B60	-	-		-

Table 2.8.3 - Pin Assignment for Expansion Port J6 _AB

Expansion port J6 _CD

The pin assignments for the J6_CD expansion port are shown in Table 2.8.4:

J6 pin	Signal name	FPGA numbers	pin	Level Standard	J6 pin	Signal name	FPGA numbers	pin	Level Standard
C1	GND	-		GND	D1	GND	-		GND
C2	104_CLK1_P	J11		1.2V	D2	104_CLK1_N	H11		1.2V
C3	GND	-		GND	D3	GND	-		GND
C4	GND	-		GND	D4	GND	-		GND
C5	104_TX0_P	F9		1.2V	D5	104_TX0_N	E9		1.2V
C6	GND	-		GND	D6	GND	-		GND
C7	GND	-		GND	D7	GND	-		GND
C8	104_TX1_P	F11		1.2V	D8	104_TX1_N	E11		1.2V
C9	GND	-		GND	D9	GND	-		GND
C10	GND	-		GND	D10	GND	-		GND
C11	104_TX2_P	F13		1.2V	D11	104_TX2_N	E13		1.2V
C12	GND	-		GND	D12	GND	-		GND
C13	GND	-		GND	D13	GND	-		GND
C14	104_TX3_P	F15		1.2V	D14	104_TX3_N	E15		1.2V
C15	GND	-		GND	D15	GND	-		GND
C16	GND	-		GND	D16	GND	-		GND

J6 pin	Signal name	FPGA numbers	pin	Level Standard	J6 pin	Signal name	FPGA numbers	pin	Level Standard
C17	105_CLK1_P	J17		1.2V	D17	105_CLK1_N	H17		1.2V
C18	GND	-		GND	D18	GND	-		GND
C19	GND	-		GND	D19	GND	-		GND
C20	105_TX0_P	F17		1.2V	D20	105_TX0_N	E17		1.2V
C21	GND	-		GND	D21	GND	-		GND
C22	GND	-		GND	D22	GND	-		GND
C23	105_TX1_P	F19		1.2V	D23	105_TX1_N	E19		1.2V
C24	GND	-		GND	D24	GND	-		GND
C25	GND	-		GND	D25	GND	-		GND
C26	105_TX2_P	F21		1.2V	D26	105_TX2_N	E21		1.2V
C27	GND	-		GND	D27	GND	-		GND
C28	GND	-		GND	D28	GND	-		GND
C29	105_TX3_P	F23		1.2V	D29	105_TX3_N	E23		1.2V
C30	GND	-		GND	D30	GND	-		GND
C31	-	-		-	D31	-	-		-
C32	-	-		-	D32	-	-		-
C33	GND	-		GND	D33	GND	-		GND
C34	B400_L2_N	E34		3.3V	D34	B400_L0_N	F36		3.3V
C35	B400_L2_P	E35		3.3V	D35	B400_L0_P	F37		3.3V
C36	GND	-		GND	D36	GND	-		GND
C37	B400_L4_N	D32		3.3V	D37	B400_L3_N	D33		3.3V
C38	B400_L4_P	E33		3.3V	D38	B400_L3_P	D34		3.3V
C39	GND	-		GND	D39	GND	-		GND
C40	B400_L8_N	C29		3.3V	D40	B401_L5_N	C34		3.3V
C41	B400_L8_P	D29		3.3V	D41	B401_L5_P	C35		3.3V
C42	GND	-		GND	D42	GND	-		GND
C43	B401_L3_N	A35		3.3V	D43	B401_L2_N	A36		3.3V

J6 pin	Signal name	FPGA numbers	pin	Level Standard	J6 pin	Signal name	FPGA numbers	pin	Level Standard
C44	B401_L3_P	B35		3.3V	D44	B401_L2_P	B37		3.3V
C45	GND	-		GND	D45	GND	-		GND
C46	B401_L1_N	C36		3.3V	D46	B401_L0_N	C37		3.3V
C47	B401_L1_P	D36		3.3V	D47	B401_L0_P	D37		3.3V
C48	GND	-		GND	D48	GND	-		GND
C49	B711_L2_N	H28		1.2V	D49	B711_L3_N	J30		1.2V
C50	B711_L2_P	J28		1.2V	D50	B711_L3_P	H29		1.2V
C51	GND	-		GND	D51	GND	-		GND
C52	B711_L4_N	H32		1.2V	D52	B711_L5_N	J31		1.2V
C53	B711_L4_P	H31		1.2V	D53	B711_L5_P	K30		1.2V
C54	GND	-		GND	D54	GND	-		GND
C55	B711_L9_N	K33		1.2V	D55	B711_L1_N	K29		1.2V
C56	B711_L9_P	K32		1.2V	D56	B711_L1_P	L29		1.2V
C57	GND	-		GND	D57	GND	-		GND
C58	B711_L7_N	M31		1.2V	D58	B711_L0_N	L28		1.2V
C59	B711_L7_P	M30		1.2V	D59	B711_L0_P	M28		1.2V
C60	-	-		-	D60	-	-		-

Table 2.8.4 - Expansion Port J6 _ CD Pin Assignment

Expansion port J7

240- pin connector J7 is used to connect to the PL terminal HP IO of the FPGA on the carrier board . The pin assignment of the J7_AB expansion port is shown in Table 2.8.5 :

J7 pin	Signal name	FPGA numbers	pin	Level Standard	J7 pin	Signal name	FPGA numbers	pin	Level Standard
A1	B710_L12_N	P31		1.2V	B1	B710_L10_N	U32		1.2V
A2	B710_L12_P	N30		1.2V	B2	B710_L10_P	U31		1.2V
A3	GND	-		GND	B3	GND	-		GND
A4	B710_L7_N	P34		1.2V	B4	B710_L8_N	N32		1.2V
A5	B710_L7_P	N33		1.2V	B5	B710_L8_P	P32		1.2V
A6	GND	-		GND	B6	GND	-		GND

J7 pin	Signal name	FPGA numbers	pin	Level Standard	J7 pin	Signal name	FPGA numbers	pin	Level Standard
A7	B710_L5_N	U35		1.2V	B7	B710_L2_N	N35		1.2V
A8	B710_L5_P	U34		1.2V	B8	B710_L2_P	P35		1.2V
A9	GND	-		GND	B9	GND	-		GND
A10	B710_L1_N	P37		1.2V	B10	B710_L4_N	T36		1.2V
A11	B710_L1_P	N36		1.2V	B11	B710_L4_P	T35		1.2V
A12	GND	-		GND	B12	GND	-		GND
A13	B709_L9_N	V34		1.2V	B13	B709_L7_N	V31		1.2V
A14	B709_L9_P	V33		1.2V	B14	B709_L7_P	W30		1.2V
A15	GND	-		GND	B15	GND	-		GND
A16	B709_L6_N	Y32		1.2V	B16	B709_L8_N	W33		1.2V
A17	B709_L6_P	Y31		1.2V	B17	B709_L8_P	W32		1.2V
A18	GND	-		GND	B18	GND	-		GND
A19	B709_L11_N	Y35		1.2V	B19	B709_L15_N	AA37		1.2V
A20	B709_L11_P	Y34		1.2V	B20	B709_L15_P	AA36		1.2V
A21	GND	-		GND	B21	GND	-		GND
A22	B709_L10_N	AA34		1.2V	B22	B708_L10_N	AF32		1.2V
A23	B709_L10_P	AA33		1.2V	B23	B708_L10_P	AF31		1.2V
A24	GND	-		GND	B24	GND	-		GND
A25	B708_L7_N	AB33		1.2V	B25	B708_L6_N	AC35		1.2V
A26	B708_L7_P	AB32		1.2V	B26	B708_L6_P	AC34		1.2V
A27	GND	-		GND	B27	GND	-		GND
A28	B708_L5_N	AD34		1.2V	B28	B708_L3_N	AF37		1.2V
A29	B708_L5_P	AD33		1.2V	B29	B708_L3_P	AE36		1.2V
A30	GND	-		GND	B30	GND	-		GND
A31	B708_L8_N	AC32		1.2V	B31	B708_L4_N	AF35		1.2V
A32	B708_L8_P	AC31		1.2V	B32	B708_L4_P	AF34		1.2V
A33	GND	-		GND	B33	GND	-		GND
A34	B708_L15_N	AF29		1.2V	B34	B708_L1_N	AB36		1.2V
A35	B708_L15_P	AG28		1.2V	B35	B708_L1_P	AB35		1.2V

J7 pin	Signal name	FPGA numbers	pin	Level Standard	J7 pin	Signal name	FPGA numbers	pin	Level Standard
A36	GND	-		GND	B36	GND	-		GND
A37	B707_L0_N	AK30		1.2V	B37	B707_L4_N	AH32		1.2V
A38	B707_L0_P	AL30		1.2V	B38	B707_L4_P	AG31		1.2V
A39	GND	-		GND	B39	GND	-		GND
A40	B707_L5_N	AH33		1.2V	B40	B707_L8_N	AK34		1.2V
A41	B707_L5_P	AJ32		1.2V	B41	B707_L8_P	AK33		1.2V
A42	GND	-		GND	B42	GND	-		GND
A43	B707_L11_N	AG37		1.2V	B43	B707_L12_N	AH36		1.2V
A44	B707_L11_P	AG36		1.2V	B44	B707_L12_P	AH35		1.2V
A45	GND	-		GND	B45	GND	-		GND
A46	B707_L13_N	AJ37		1.2V	B46	B707_L14_N	AK36		1.2V
A47	B707_L13_P	AK37		1.2V	B47	B707_L14_P	AL35		1.2V
A48	GND	-		GND	B48	GND	-		GND
A49	B706_L11_N	AM31		1.2V	B49	B706_L10_N	AN33		1.2V
A50	B706_L11_P	AN31		1.2V	B50	B706_L10_P	AM32		1.2V
A51	GND	-		GND	B51	GND	-		GND
A52	B706_L3_N	AN37		1.2V	B52	B706_L9_N	AP33		1.2V
A53	B706_L3_P	AN36		1.2V	B53	B706_L9_P	AP32		1.2V
A54	GND	-		GND	B54	GND	-		GND
A55	B706_L5_N	AR35		1.2V	B55	B706_L1_N	AT37		1.2V
A56	B706_L5_P	AR34		1.2V	B56	B706_L1_P	AT36		1.2V
A57	GND	-		GND	B57	GND	-		GND
A58	B706_L0_N	AU36		1.2V	B58	B706_L6_N	AT34		1.2V
A59	B706_L0_P	AU35		1.2V	B59	B706_L6_P	AT33		1.2V
A60	-	-		-	B60	-	-		-

Table 2.8.5 - Expansion Port J7 _AB Pin Assignment

Expansion port J7 _CD

The pin assignments for the J7_CD expansion port are shown in Table 2.8.6:

J7 pin	Signal name	FPGA numbers	pin	Level Standard	J7 pin	Signal name	FPGA numbers	pin	Level Standard
C1	B710_L13_N	N29		1.2V	D1	B710_L14_N	P28		1.2V
C2	B710_L13_P	P29		1.2V	D2	B710_L14_P	R28		1.2V
C3	GND	-		GND	D3	GND	-		GND
C4	B710_L11_N	R31		1.2V	D4	B710_L15_N	T30		1.2V
C5	B710_L11_P	R30		1.2V	D5	B710_L15_P	T29		1.2V
C6	GND	-		GND	D6	GND	-		GND
C7	B710_L6_N	R34		1.2V	D7	B710_L9_N	T33		1.2V
C8	B710_L6_P	R33		1.2V	D8	B710_L9_P	T32		1.2V
C9	GND	-		GND	D9	GND	-		GND
C10	B710_L3_N	R37		1.2V	D10	B710_L0_N	M37		1.2V
C11	B710_L3_P	R36		1.2V	D11	B710_L0_P	M36		1.2V
C12	GND	-		GND	D12	GND	-		GND
C13	B709_L4_N	V30		1.2V	D13	B709_L3_N	U28		1.2V
C14	B709_L4_P	U29		1.2V	D14	B709_L3_P	V28		1.2V
C15	GND	-		GND	D15	GND	-		GND
C16	B709_L13_N	U37		1.2V	D16	B709_L2_N	W29		1.2V
C17	B709_L13_P	V37		1.2V	D17	B709_L2_P	Y29		1.2V
C18	GND	-		GND	D18	GND	-		GND
C19	B709_L12_N	V36		1.2V	D19	B709_L14_N	Y37		1.2V
C20	B709_L12_P	W35		1.2V	D20	B709_L14_P	W36		1.2V
C21	GND	-		GND	D21	GND	-		GND
C22	B709_L5_N	AA31		1.2V	D22	B709_L0_N	AB30		1.2V
C23	B709_L5_P	AA30		1.2V	D23	B709_L0_P	AB29		1.2V
C24	GND	-		GND	D24	GND	-		GND
C25	B708_L14_N	AE29		1.2V	D25	B709_L1_N	Y28		1.2V
C26	B708_L14_P	AF28		1.2V	D26	B709_L1_P	AA28		1.2V
C27	GND	-		GND	D27	GND	-		GND

J7 pin	Signal name	FPGA numbers	pin	Level Standard	J7 pin	Signal name	FPGA numbers	pin	Level Standard
C28	B708_L9_N	AE33		1.2V	D28	B708_L11_N	AD31		1.2V
C29	B708_L9_P	AE32		1.2V	D29	B708_L11_P	AE30		1.2V
C30	GND	-		GND	D30	GND	-		GND
C31	B708_L12_N	AD30		1.2V	D31	B708_L13_N	AC28		1.2V
C32	B708_L12_P	AC29		1.2V	D32	B708_L13_P	AD28		1.2V
C33	GND	-		GND	D33	GND	-		GND
C34	B708_L0_N	AC37		1.2V	D34	B708_L2_N	AD36		1.2V
C35	B708_L0_P	AD37		1.2V	D35	B708_L2_P	AE35		1.2V
C36	GND	-		GND	D36	GND	-		GND
C37	B707_L10_N	AG34		1.2V	D37	B707_L1_N	AH29		1.2V
C38	B707_L10_P	AG33		1.2V	D38	B707_L1_P	AJ29		1.2V
C39	GND	-		GND	D39	GND	-		GND
C40	B707_L6_N	AL33		1.2V	D40	B707_L2_N	AG30		1.2V
C41	B707_L6_P	AL32		1.2V	D41	B707_L2_P	AH30		1.2V
C42	GND	-		GND	D42	GND	-		GND
C43	B707_L9_N	AJ35		1.2V	D43	B707_L3_N	AJ31		1.2V
C44	B707_L9_P	AJ34		1.2V	D44	B707_L3_P	AK31		1.2V
C45	GND	-		GND	D45	GND	-		GND
C46	B707_L15_N	AM37		1.2V	D46	B707_L7_N	AM35		1.2V
C47	B707_L15_P	AL36		1.2V	D47	B707_L7_P	AM34		1.2V
C48	GND	-		GND	D48	GND	-		GND
C49	B706_L4_N	AP35		1.2V	D49	B706_L12_N	AN30		1.2V
C50	B706_L4_P	AN34		1.2V	D50	B706_L12_P	AP29		1.2V
C51	GND	-		GND	D51	GND	-		GND
C52	B706_L13_N	AP30		1.2V	D52	B706_L8_N	AR32		1.2V
C53	B706_L13_P	AR29		1.2V	D53	B706_L8_P	AR31		1.2V
C54	GND	-		GND	D54	GND	-		GND

J7 pin	Signal name	FPGA numbers	pin	Level Standard	J7 pin	Signal name	FPGA numbers	pin	Level Standard
C55	B706_L2_N	AR37		1.2V	D55	B706_L7_N	AU33		1.2V
C56	B706_L2_P	AP36		1.2V	D56	B706_L7_P	AU32		1.2V
C57	GND	-		GND	D57	GND	-		GND
C58	B706_L14_N	AT31		1.2V	D58	B706_L15_N	AU30		1.2V
C59	B706_L14_P	AT30		1.2V	D59	B706_L15_P	AU29		1.2V
C60	-	-		-	D60	-	-		-

Table 2.8.6 - Expansion Port J7 _ CD Pin Assignment

2.9 Structural Diagram

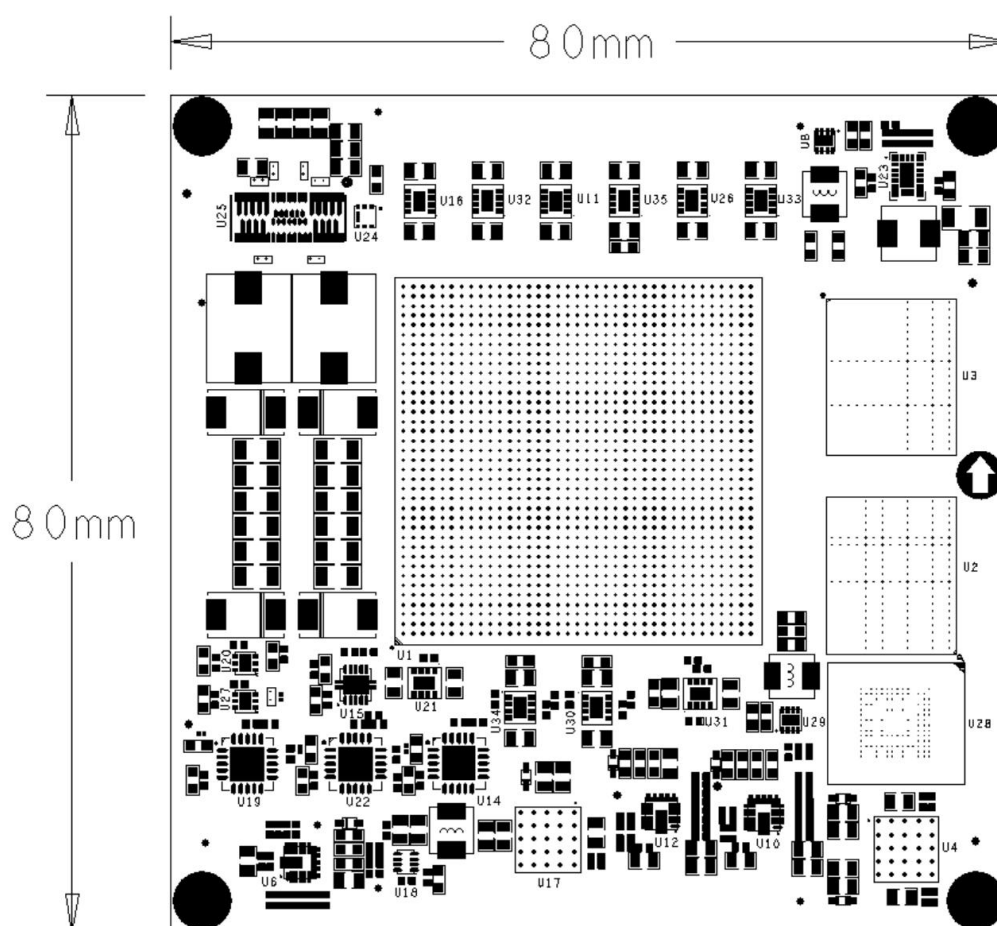


Figure 2.9.1 - Top View

Chapter3 AXVM2152 Carrier Board

3.1 Introduction

Through the preceding functional overview, we can understand the functions of the carrier board.

- 1 Gigabit Ethernet RJ-45 interface
- PCIe 4.0 x8 / PCIe 5.0 x4 interface
- 1-channel USB UART debugging interface
- 1 USB 2.0 port
- 1 LVDS display interface
- 1- channel 4-LANE MIPI camera interface
- 1-way FMC+ interface
- 1-way Micro SD card slot
- 1-channel EEPROM
- 1-channel temperature sensor
- JTAG debug port
- 2- channel CANFD communication interface
- 1-channel 40 -pin expansion port
- Buttons and LED lights

3.2 Gigabit Ethernet

The AXVM2152 expansion board features a Gigabit Ethernet interface connected to the PS device. It provides network communication services through JL Semi's industrial-grade Ethernet GPHY chip (JL2121-N040I). The JL2121 chip supports 10/100/1000 Mbps network transmission rates and communicates with the FPGA's MAC layer via the RGMII interface. The JL2121D variant supports MDI/MDX adaptation, various speed adaptations, Master/Slave adaptation, and MDIO bus-based PHY register management.

Upon power-on, the JL2121 detects the voltage levels of specific I/O pins to determine its operating mode. Table 3.2.1 outlines the default configuration settings for the GPHY chip after power-on.

Configure Pin	illustrate	Configuration value
RXD3_ADR0	PHY address in MDIO/MDC mode	PHY Address is 001

RXC_ADR1 RXCTL_ADR2		
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

Table 3.2.1 - Default Configuration Values for PHY Chip

When the network is connected to Gigabit Ethernet, the FPGA and PHY chip JL2121 communicate via the RGMII bus for data transmission. The transmission clock is 125MHz, and the data is sampled on the rising and falling edges of the clock.

When the network is connected to a 100 Mbps Ethernet network, data transmission between the FPGA and the JL2121 PHY chip is conducted via the RMII bus, with a transmission clock of 25 MHz. Data is sampled on both the rising and falling edges of the clock. A schematic diagram of the Gigabit Ethernet design is shown in Figure 3.2.1 .

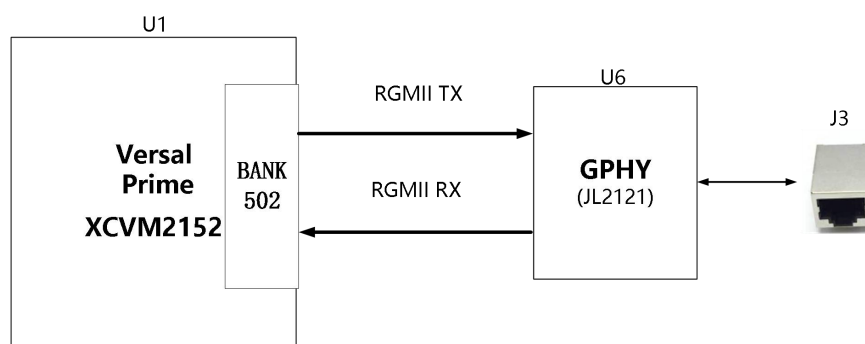


Figure 3.2.1 - Schematic diagram of Gigabit Ethernet interface design

Gigabit Ethernet pin assignments are as follows:

Signal name	pin name	pin number	Remark
PHY1_TXCK	LPD_MIO12	AG5	Ethernet 1RGMII Transmit Clock
PHY1_TXD0	LPD_MIO13	AF5	Ethernet 1 transmits data bit 0
PHY1_TXD1	LPD_MIO14	AE5	Ethernet 1 transmits data bit 1
PHY1_TXD2	LPD_MIO15	AD4	Ethernet 1 transmits data bit 2
PHY1_TXD3	LPD_MIO16	AE4	Ethernet 1 transmits data bit 3
PHY1_TXCTL	LPD_MIO17	AF3	Ethernet 1 sends enable signal
PHY1_RXCK	LPD_MIO18	AE3	Ethernet 1RGMII Receive Clock
PHY1_RXD0	LPD_MIO19	AD3	Ethernet 1 Receive Data Bit0
PHY1_RXD1	LPD_MIO20	AD2	Ethernet 1 Receive Data Bit 1
PHY1_RXD2	LPD_MIO21	AF2	Ethernet 1 receives data Bit 2
PHY1_RXD3	LPD_MIO22	AF1	Ethernet 1 receives data Bit 3

Signal name	pin name	pin number	Remark
PHY1_RXCTL	LPD_MIO23	AE1	Ethernet 1 receive data valid signal
PHY1_MDIO	LPD_MIO25	AC1	Ethernet 1MDIO Management Data
PHY1_MDC	LPD_MIO24	AD1	Ethernet 1MDIO Management Clock
PHY1_RESET	LPD_MIO11	AH5	Ethernet 1 reset signal

Table 3.2.2 - Gigabit Ethernet Pin Assignment

3.3 PCIe 4.0 x8/PCIe 5.0 x4

The AXVM2152 carrier board provides an industrial-grade high-speed data transfer PCIe 4.0 x 8/PCIe 5.0 x 4 interface . The PCIe card's form factor conforms to the standard PCIe card electrical specifications and can be used directly in a standard PC's x 8 PCIe slot.

The PCIe interface's transmit and receive signals are directly connected to the FPGA's GTY transceiver. The four-channel TX and RX signals are connected to the FPGA in a differential signal configuration, with a single-channel communication rate of up to 16 Gbps bandwidth. The PCIe reference clock is provided to the development board by the PC's PCIe slot, with a reference clock frequency of 100MHz.

The design schematic of the PCIe interface of the development board is shown in Figure 3.3.1 below , where the TX transmit signal and the reference clock CLK signal are connected in AC coupling mode.

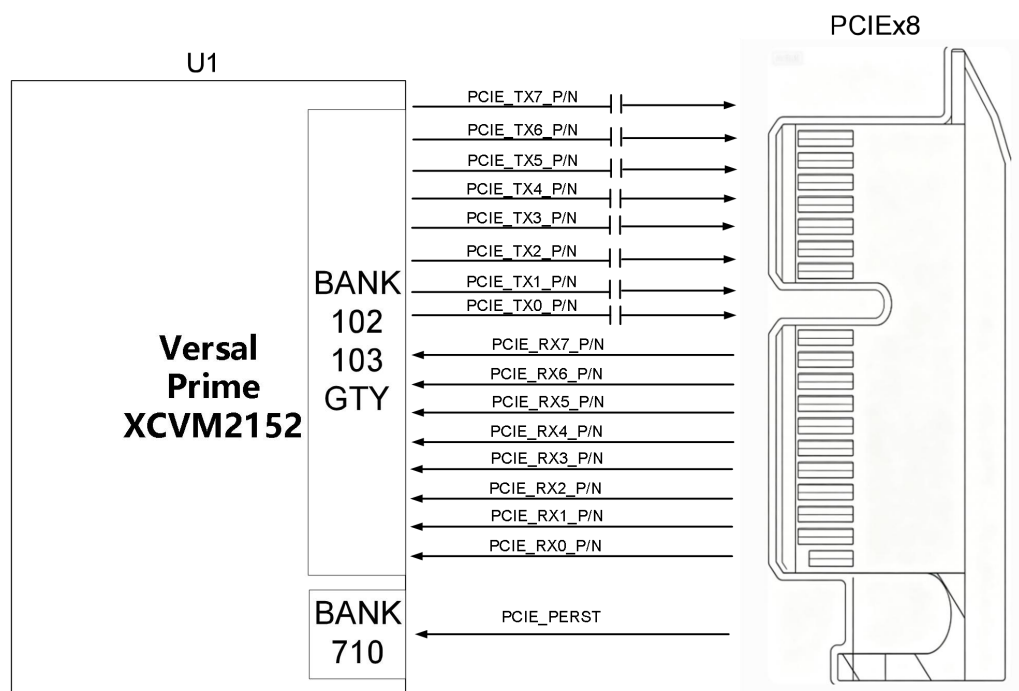


Figure 3.3.1 - PCIe x8 design schematic

The pin assignments for the PCIe x4 interface FPGA are as follows:

Network Name	FPGA pin names	FPGA pin numbers	Remark
PCIE_RX0_P	103_RX3_P	A4	PCle Channel 0 Data Receive Positive
PCIE_RX0_N	103_RX3_N	A3	PCle channel 0 data reception (Negative)
PCIE_RX1_P	103_RX2_P	B2	PCle Channel 1 Data Receive Positive
PCIE_RX1_N	103_RX2_N	B1	PCle Channel 1 Data Receiver (Negative)
PCIE_RX2_P	103_RX1_P	C4	PCle Channel 2 Data Receive Positive
PCIE_RX2_N	103_RX1_N	C3	PCle Channel 2 Data Receiver (Negative)
PCIE_RX3_P	103_RX0_P	D2	PCle Channel 3 Data Reception Positive
PCIE_RX3_N	103_RX0_N	D1	PCle Channel 3 Data Receiver (Negative)
PCle RX 4 _P	102_RX3_P	F2	PCle Channel 4 Data Receive Positive
PCIE_RX 4 _N	102_RX3_N	F1	PCle Channel 4 Data Receive Negative
PCle RX 5 _P	102_RX2_P	H2	PCle lane 5 data reception Positive
PCIE_RX5_N	102_RX2_N	H1	PCle Channel 5 Data Receiver (Negative)
PCIE_RX 6_P	102_RX1_P	K2	PCle lane 6 data reception Positive
PCIE_RX 6_N	102_RX1_N	K1	PCle Channel 6 Data Receiver (Negative)
PCle RX 7 _P	102_RX0_P	M2	Positive data reception on PCle lane 7
PCIE_RX 7_N	102_RX0_N	M1	PCle lane 7 data reception Negative
PCIE_TX0_P	103_TX3_P	B7	PCle Channel 0 Data Transmission Positive
PCIE_TX0_N	103_TX3_N	B6	PCle channel 0 data transmission Negative
PCIE_TX1_P	103_TX2_P	D7	PCle Channel 1 Data Transmission Positive
PCIE_TX1_N	103_TX2_N	D6	PCle Channel 1 Data Transmission Negative
PCIE_TX2_P	103_TX1_P	E5	PCle Channel 2 Data Transmission Positive
PCIE_TX2_N	103_TX1_N	E4	PCle Channel 2 Data Transmission Negative
PCIE_TX3_P	103_TX0_P	F7	PCle Channel 3 Data Transmission Positive
PCIE_TX3_N	103_TX0_N	F6	PCle Channel 3 Data Transmission Negative
PCIE_TX 4 _P	102_TX3_P	G5	PCle Channel 4 Data Transmission Positive
PCIE_TX 4 _N	102_TX3_N	G4	PCle Channel 4 Data Transmission Negative
PCIE_TX 5 _P	102_TX2_P	J5	PCle Channel 5 Data Transmission Positive

Network Name	FPGA pin names	FPGA pin numbers	Remark
PCIE_TX 5 _N	102_TX2_N	J4	PCle Channel 5 Data Transmission Negative
PCIE_TX 6 _P	102_TX1_P	L5	PCle Channel 6 Data Transmission Positive
PCIE_TX 6 _N	102_TX1_N	L4	PCle Channel 6 Data Transmission Negative
PCIE_TX 7 _P	102_TX0_P	N5	PCle Channel 7 Data Transmission Positive
PCIE_TX 7 _N	102_TX0_N	N4	PCle Channel 7 Data Transmission Negative
PCIE_CLK 0 _P	102_CLK0_P	N9	PCle reference clock 0 Positive
PCIE_CLK 0 _N	102_CLK0_N	N8	PCle Reference Clock 0 Negative
PCIE_CLK 1 _P	103_CLK0_P	K7	PCle Reference Clock 1 Positive
PCIE_CLK 1 _N	103_CLK0_N	K6	PCle Reference Clock 1 Negative
PCIE_PERST	B710_L0_N	M37	PCle reset signal

Table 3.3.1 - FPGA Pin Assignments for PCIe x8 Interface

3.4 USB to Serial Port

The AXVM2152 carrier board is equipped with a UART-to-USB interface connected to the PS (Power Supply). The converter chip is the Silicon Labs CP2102GM USB- UART chip , and the USB interface is a Type-C interface, allowing it to be connected to the PC 's USB port for serial data communication using a single USB cable. A schematic diagram of the USB UART circuit design is shown in Figure 3.4.1 .

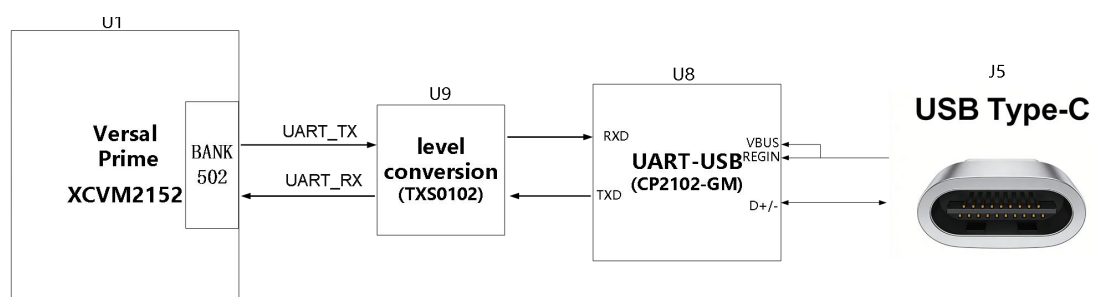


Figure 3.4.1 - Schematic diagram of USB to serial port adapter

FPGA pin assignment for UART to serial port conversion:

Signal name	FPGA pin names	FPGA pin numbers	Remark
PS_UART0_RX	LPD_MIO8	AF6	UART data input
PS_UART0_TX	LPD_MIO9	AH6	UART data output

Table 3.4.1 - FPGA Pin Assignments for UART to Serial Port

3.5 USB 2.0

The AXVM2152 carrier board has one USB 2.0 port that supports HOST mode. The USB 2.0 port connects to an external USB3320C chip via the ULPI interface to achieve high-speed USB 2.0 data communication.

The USB interface is USB. The Type- C interface allows users to connect different USB Slave peripherals simultaneously (such as a USB mouse, keyboard, or flash drive). A diagram of a USB 2.0 connection is shown in Figure 3.5.1 .

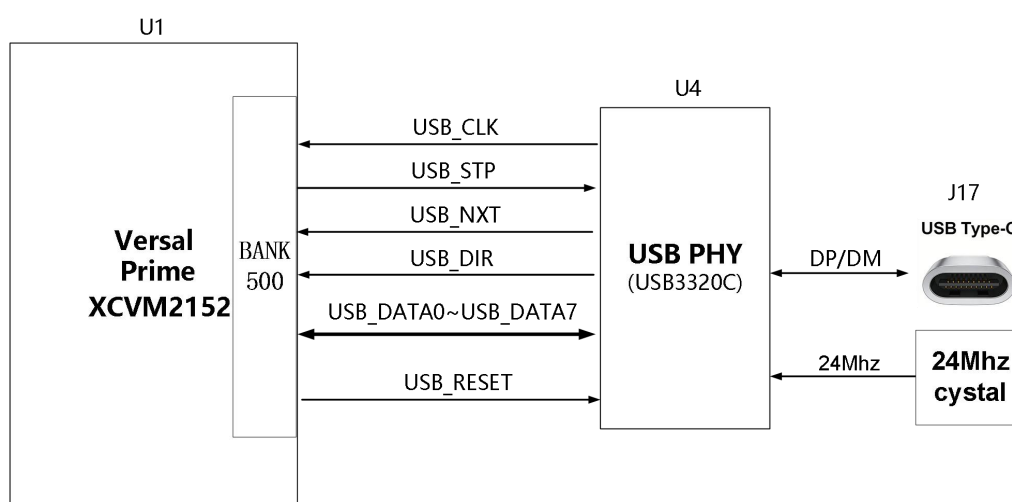


Figure 3.5.1 - Schematic diagram of USB 2.0 interface

USB interface pin assignment:

Signal name	pin name	pin number	Remark
USB_DATA0	PS_MIO14	R3	USB 2.0 data bit 0
USB_DATA1	PS_MIO15	T3	USB 2.0 data bit 1
USB_DATA2	PS_MIO16	U3	USB 2.0 data bit 2
USB_DATA3	PS_MIO17	W3	USB 2.0 data bit 3
USB_DATA4	PS_MIO19	U2	USB 2.0 data bit 4
USB_DATA5	PS_MIO20	T2	USB 2.0 data bit 5
USB_DATA6	PS_MIO21	P2	USB 2.0 data bit 6
USB_DATA7	PS_MIO22	P1	USB 2.0 data bit 7
USB_STP	PS_MIO24	T1	USB 2.0 stop signal
USB_DIR	PS_MIO23	R1	USB 2.0 data direction signal
USB_CLK	PS_MIO18	V2	USB 2.0 clock signal

USB_NXT	PS_MIO25	V1	USB 2.0 next data signal
USB_RESET_N	PS_MIO13	R4	USB 2.0 reset signal

Table 3.5.1 - USB Interface Pin Assignment

3.6 LVDS Display

The AXVM2152 carrier board includes an LVDS display interface, which can be used to connect our 7-inch display module (AN7000). The LVDS interface is a 40-pin FPC connector with 4 pairs of LVDS data and 1 pair of clock signals. Other control signals are connected to the differential I/O pins of the BANK 400 via a level conversion chip , with a voltage standard of 3.3V .

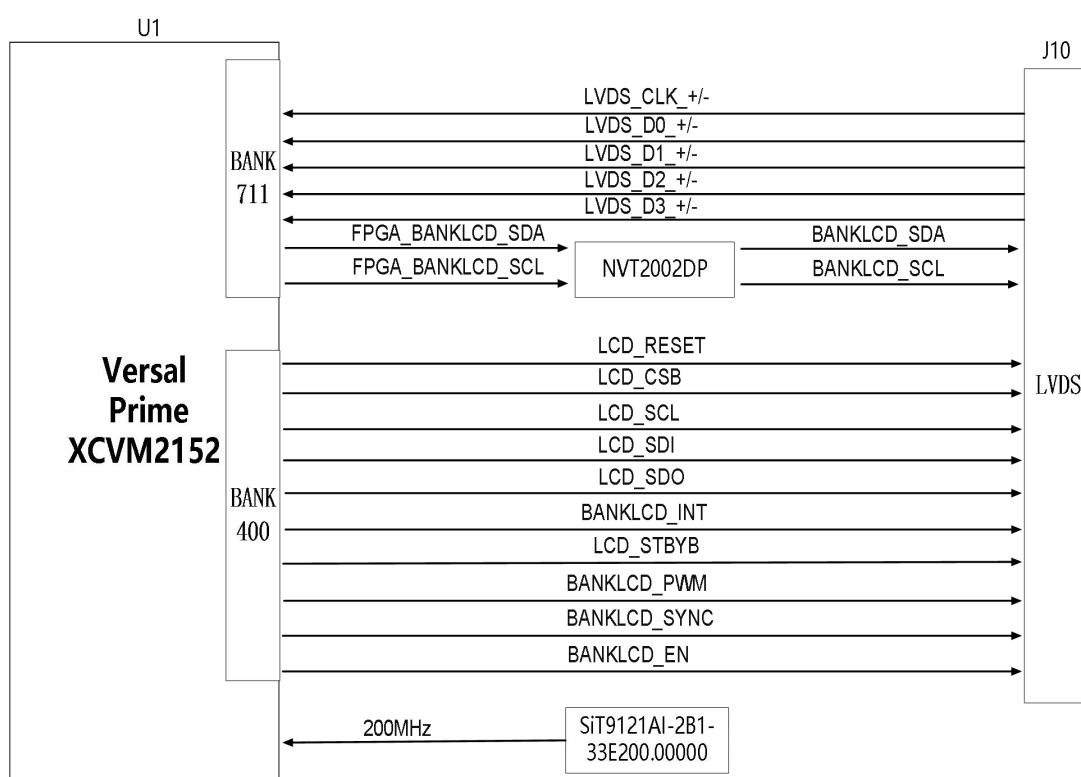


Figure 3.6.1 - LVDS Interface Design Schematic

LVDS Interface Pin Assignment

Signal name	pin name	pin number	Remark
LVDS_CLK-	B711_L9_N	K33	LVDS screen input clock negative
LVDS_CLK+	B711_L9_P	K32	LVDS screen input clock positive
LVDS_D0-	B711_L12_N	L35	LVDS screen input data DATA0 negative
LVDS_D0+	B711_L12_P	L34	DATA0 input to the LVDS screen is positive
LVDS_D1-	B711_L10_N	J34	DATA1 input data on the LVDS screen is negative

Signal name	pin name	pin number	Remark
LVDS_D1+	B711_L10_P	J33	DATA1 input to the LVDS screen is positive
LVDS_D2-	B711_L11_N	H35	The data input to the LVDS screen is DATA2 negative.
LVDS_D2+	B711_L11_P	H34	The data DATA2 input to the LVDS screen is positive.
LVDS_D3-	B711_L14_N	J36	LVDS screen input data DATA3 negative
LVDS_D3+	B711_L14_P	K35	DATA3 input to the LVDS screen is positive
FPGA_LCD_SDI	B400_L10_P	F28	LCD screen serial interface address and SPI data input
FPGA_LCD_CSB	B400_L6_N	E31	LCD screen serial interface chip SPI chip select signal
FPGA_LCD_SCL	B400_L6_P	F31	LCD screen serial interface SPI clock
FPGA_LCD_SDO	B400_L10_N	E28	LCD screen serial interface SPI data output
FPGA_LCD_RESET	B400_L2_P	E35	LCD screen reset signal
FPGA_LCD_STBYB	B400_L2_N	E34	LCD screen mode setting signal
FPGA_BANKLCD_SDA	B711_L15_N	H37	Backlight I2C data
FPGA_BANKLCD_SCL	B711_L15_P	J37	Backlit I2C Clock
FPGA_BANKLCD_INT	B400_L7_P	E30	Backlight fault interruption signal
FPGA_BANKLCD_EN	B400_L3_N	D33	Backlight enable signal
FPGA_BANKLCD_PWM	B400_L3_P	D34	Backlight brightness adjustment signal
FPGA_BANKLCD_SYNC	B400_L7_N	D31	Backlight Synchronous Boost Input
LVDS_CLK_N	B711_L13_N	L37	FPGA input clock negative
LVDS_CLK_P	B711_L13_P	K36	FPGA input clock positive

Table 3.6.1 - LVDS Interface Pin Assignment

3.7 MIPI

The AXVM2152 carrier board features a MIPI 4-Lane camera interface for connecting our MIPI OS05A20 camera module (AN5020). The MIPI interface employs a 20-pin FPC connector with four data lanes and one clock pair, connected to the differential IO pins of BANK702 at a voltage level of 1.2 V; other control signals are routed via a voltage converter to the IO pins of BANK711, operating at 1.5 V.

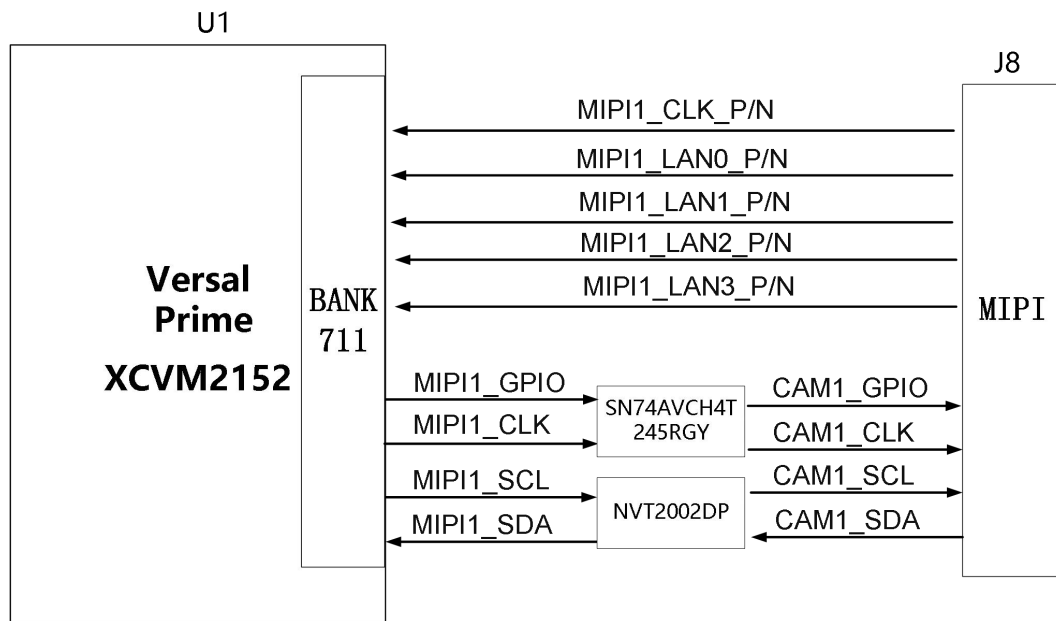


Figure 3.8.1 - MIPI Interface Design Schematic

MIPI Interface Pin Assignment

Signal name	Pin name	Pin number	Remark
MIPI1_CLK_N	B711_L1_N	K29	MIPI1 input clock negative
MIPI1_CLK_P	B711_L1_P	L29	MIPI1 input clock positive
MIPI1_LAN0_N	B711_L2_N	H28	MIPI1 input data LANE0 negative
MIPI1_LAN0_P	B711_L2_P	J28	MIPI1 input data LANE0 is positive
MIPI1_LAN1_N	B711_L3_N	J30	MIPI1 input data LANE1 negative
MIPI1_LAN1_P	B711_L3_P	H29	MIPI1 input data LANE1 is positive
MIPI1_LAN2_N	B711_L5_N	J31	MIPI1 input data LANE2 negative
MIPI1_LAN2_P	B711_L5_P	K30	MIPI1 input data LANE2 is positive
MIPI1_LAN3_N	B711_L4_N	H32	MIPI1 input data LANE3 negative
MIPI1_LAN3_P	B711_L4_P	H31	MIPI1 input data LANE3 is positive
MIPI1_SDA	B711_L8_N	M34	MIPI1 camera I2C data
MIPI1_SCL	B711_L8_P	M33	MIPI1 camera's I2C clock
MIPI1_GPIO	B711_L7_N	M31	GPIO control of MIPI1 camera
MIPI1_CLK	B711_L7_P	M30	Clock input of MIPI1 camera

Table 3.7.1 - MIPI Interface Pin Assignment

3.8 FMC+

The AXVM2152 development board has one standard FMC + interface , which can be connected to various FMC modules from Xilinx or Alinx (HDMI input/output modules, binocular camera modules, high-speed AD modules, etc.).

The FMC+ HPC expansion port includes 34 pairs of LA signal differential pairs, 4 pairs of clock signals, 24 pairs of HA signals, and 18 pairs of HB signals, which are connected to FPGA chips BANK 706 , BANK 707 , BANK 708 , BANK 709, and BANK 710 , respectively ; the default voltage level is 1.2V . Eight high -speed GTM transceiver signals are connected to the I/O pins of FPGA chips BANK 104 ~BANK 105. The schematic diagram of the FPGA and FMC 1+ HPC connector is shown in Figure 3.8.1 .

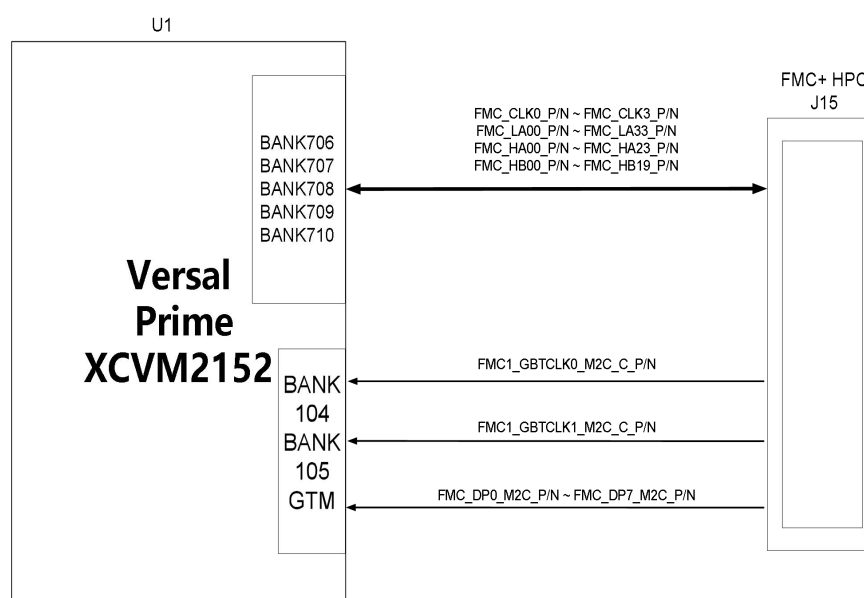


Figure 3.8.1- FMC+ HPC Connection Diagram

The pin assignment for the FMC+ HPC connector is as follows:

Pin number	signal name	FPGA pin names	FPGA pins	Remark
H5	FMC1_CLK0_N	B709_L9_N	V34	FMC Channel 0 Input Reference Clock N
H4	FMC1_CLK0_P	B709_L9_P	V33	FMC Input Reference Clock P (Channel 0)
G3	FMC1_CLK1_N	B709_L13_N	U37	FMC Input Reference Clock N
G2	FMC1_CLK1_P	B709_L13_P	V37	FMC Input Reference Clock P
G7	FMC1_LA00_CC_N	B710_L3_N	R37	FMC LA 0th data (clock) N
G6	FMC1_LA00_CC_P	B710_L3_P	R36	FMC LA 0th data (clock) P
D9	FMC1_LA01_CC_N	B710_L1_N	P37	FMC LA First Channel Data (Clock) N

Pin number	signal name	FPGA pin names	FPGA pins	Remark
D8	FMC1_LA01_CC_P	B710_L1_P	N36	FMC LA Channel 1 Data (Clock) P
H8	FMC1_LA02_N	B710_L2_N	N35	FMC LA Second Data N
H7	FMC1_LA02_P	B710_L2_P	P35	FMC LA Second Data P
G10	FMC1_LA03_N	B710_L7_N	P34	FMC LA 3rd data channel N
G9	FMC1_LA03_P	B710_L7_P	N33	FMC LA 3rd channel data P
H11	FMC1_LA04_N	B710_L4_N	T36	FMC LA 4th Data N
H10	FMC1_LA04_P	B710_L4_P	T35	FMC LA 4th data path P
D12	FMC1_LA05_N	B710_L5_N	U35	FMC LA 5th Data N
D11	FMC1_LA05_P	B710_L5_P	U34	FMC LA 5th Data P
C11	FMC1_LA06_N	B710_L10_N	U32	FMC LA 6th Data N
C10	FMC1_LA06_P	B710_L10_P	U31	FMC LA 6th Data P
H14	FMC1_LA07_N	B710_L12_N	P31	FMC LA 7th data channel N
H13	FMC1_LA07_P	B710_L12_P	N30	FMC LA 7th data path P
G13	FMC1_LA08_N	B710_L13_N	N29	FMC LA 8th Data N
G12	FMC1_LA08_P	B710_L13_P	P29	FMC LA 8th Data P
D15	FMC1_LA09_N	B710_L11_N	R31	FMC LA 9th Data N
D14	FMC1_LA09_P	B710_L11_P	R30	FMC LA 9th data path P
C15	FMC1_LA10_N	B710_L8_N	N32	FMC LA 10th data channel N
C14	FMC1_LA10_P	B710_L8_P	P32	FMC LA 10th data path P
H17	FMC1_LA11_N	B709_L5_N	AA31	FMC LA 11th data channel N
H16	FMC1_LA11_P	B709_L5_P	AA30	FMC LA 11th data path P
G16	FMC1_LA12_N	B710_L9_N	T33	FMC LA 12th data channel N
G15	FMC1_LA12_P	B710_L9_P	T32	FMC LA 12th data path P
D18	FMC1_LA13_N	B709_L4_N	V30	FMC LA 13th data channel N
D17	FMC1_LA13_P	B709_L4_P	U29	FMC LA 13th data path P
C19	FMC1_LA14_N	B709_L1_N	Y28	FMC LA 14th Data N
C18	FMC1_LA14_P	B709_L1_P	AA28	FMC LA 14th data path P
H20	FMC1_LA15_N	B709_L2_N	W29	FMC LA 15th Data N

Pin number	signal name	FPGA pin names	FPGA pins	Remark
H19	FMC1_LA15_P	B709_L2_P	Y29	FMC LA 15th Data P
G19	FMC1_LA16_N	B709_L3_N	U28	FMC LA 16th Data Channel N
G18	FMC1_LA16_P	B709_L3_P	V28	FMC LA 16th data path P
D21	FMC1_LA17_CC_N	B708_L3_N	AF37	FMC LA 17th data (clock) channel N
D20	FMC1_LA17_CC_P	B708_L3_P	AE36	FMC LA 17th data (clock) channel P
C23	FMC1_LA18_CC_N	B708_L1_N	AB36	FMC LA 18th data (clock) channel N
C22	FMC1_LA18_CC_P	B708_L1_P	AB35	FMC LA 18th data (clock) channel P
H23	FMC1_LA19_N	B709_L11_N	Y35	FMC LA 19th data channel N
H22	FMC1_LA19_P	B709_L11_P	Y34	FMC LA 19th data path P
G22	FMC1_LA20_N	B708_L2_N	AD36	FMC LA 20th data channel N
G21	FMC1_LA20_P	B708_L2_P	AE35	FMC LA 20th data path P
H26	FMC1_LA21_N	B707_L13_N	AJ37	FMC LA 21st data channel N
H25	FMC1_LA21_P	B707_L13_P	AK37	FMC LA 21st data path P
G25	FMC1_LA22_N	B707_L12_N	AH36	FMC LA 22nd data channel N
G24	FMC1_LA22_P	B707_L12_P	AH35	FMC LA 22nd data path P
D24	FMC1_LA23_N	B707_L11_N	AG37	FMC LA 23rd data channel N
D23	FMC1_LA23_P	B707_L11_P	AG36	FMC LA 23rd channel data P
H29	FMC1_LA24_N	B708_L4_N	AF35	FMC LA 24th data channel N
H28	FMC1_LA24_P	B708_L4_P	AF34	FMC LA 24th data path P
G28	FMC1_LA25_N	B709_L10_N	AA34	FMC LA 25th Data Channel N
G27	FMC1_LA25_P	B709_L10_P	AA33	FMC LA 25th data path P
D27	FMC1_LA26_N	B707_L9_N	AJ35	FMC LA 26th data channel N
D26	FMC1_LA26_P	B707_L9_P	AJ34	FMC LA 26th data path P
C27	FMC1_LA27_N	B707_L10_N	AG34	FMC LA 27th data channel N
C26	FMC1_LA27_P	B707_L10_P	AG33	FMC LA 27th data path P
H32	FMC1_LA28_N	B708_L5_N	AD34	FMC LA 28th data channel N
H31	FMC1_LA28_P	B708_L5_P	AD33	FMC LA 28th data path P
G31	FMC1_LA29_N	B708_L9_N	AE33	FMC LA 29th data channel N

Pin number	signal name	FPGA pin names	FPGA pins	Remark
G30	FMC1_LA29_P	B708_L9_P	AE32	FMC LA 29th data path P
H35	FMC1_LA30_N	B708_L12_N	AD30	FMC LA 30th data channel N
H34	FMC1_LA30_P	B708_L12_P	AC29	FMC LA 30th data path P
G34	FMC1_LA31_N	B708_L11_N	AD31	FMC LA 31st data channel N
G33	FMC1_LA31_P	B708_L11_P	AE30	FMC LA 31st data path P
H38	FMC1_LA32_N	B708_L13_N	AC28	FMC LA 32nd data channel N
H37	FMC1_LA32_P	B708_L13_P	AD28	FMC LA 32nd data path P
G37	FMC1_LA33_N	B708_L10_N	AF32	FMC LA 33rd data channel N
G36	FMC1_LA33_P	B708_L10_P	AF31	FMC LA 33rd channel data P
K5	FMC1_CLK2_N	B710_L15_N	T30	FMC second input reference clock N
K4	FMC1_CLK2_P	B710_L15_P	T29	FMC second input reference clock P
J3	FMC1_CLK3_N	B710_L14_N	P28	FMC 3rd Input Reference Clock N
J2	FMC1_CLK3_P	B710_L14_P	R28	FMC 3rd Input Reference Clock P
F5	FMC1_HA00_CC_N	B709_L6_N	Y32	FMC HA 0th data (clock) N
F4	FMC1_HA00_CC_P	B709_L6_P	Y31	FMC HA 0th data (clock) P
E3	FMC1_HA01_CC_N	B709_L14_N	Y37	FMC HA Channel 1 Data (Clock) N
E2	FMC1_HA01_CC_P	B709_L14_P	W36	FMC HA Channel 1 Data (Clock) P
K8	FMC1_HA02_N	B706_L12_N	AN30	FMC HA Second Data N
K7	FMC1_HA02_P	B706_L12_P	AP29	FMC HA Second Data P
J7	FMC1_HA03_N	B710_L6_N	R34	FMC HA 3rd channel data N
J6	FMC1_HA03_P	B710_L6_P	R33	FMC HA 3rd channel data P
F8	FMC1_HA04_N	B709_L7_N	V31	FMC HA 4th data path N
F7	FMC1_HA04_P	B709_L7_P	W30	FMC HA 4th data path P
E7	FMC1_HA05_N	B709_L8_N	W33	FMC HA 5th data path N
E6	FMC1_HA05_P	B709_L8_P	W32	FMC HA 5th data path P
K11	FMC1_HA06_N	B706_L0_N	AU36	FMC HA 6th data channel N
K10	FMC1_HA06_P	B706_L0_P	AU35	FMC HA 6th data path P
J10	FMC1_HA07_N	B706_L8_N	AR32	FMC HA 7th data path N

Pin number	signal name	FPGA pin names	FPGA pins	Remark
J9	FMC1_HA07_P	B706_L8_P	AR31	FMC HA 7th data path P
F11	FMC1_HA08_N	B708_L7_N	AB33	FMC HA 8th data channel N
F10	FMC1_HA08_P	B708_L7_P	AB32	FMC HA 8th data path P
E10	FMC1_HA09_N	B709_L15_N	AA37	FMC HA 9th data channel N
E9	FMC1_HA09_P	B709_L15_P	AA36	FMC HA 9th data path P
K14	FMC1_HA10_N	B708_L15_N	AF29	FMC HA 10th data channel N
K13	FMC1_HA10_P	B708_L15_P	AG28	FMC HA 10th data path P
J13	FMC1_HA11_N	B709_L12_N	V36	FMC HA 11th data channel N
J12	FMC1_HA11_P	B709_L12_P	W35	FMC HA 11th data path P
F14	FMC1_HA12_N	B708_L8_N	AC32	FMC HA 12th data channel N
F13	FMC1_HA12_P	B708_L8_P	AC31	FMC HA 12th data path P
E13	FMC1_HA13_N	B708_L6_N	AC35	FMC HA 13th data channel N
E12	FMC1_HA13_P	B708_L6_P	AC34	FMC HA 13th data path P
J16	FMC1_HA14_N	B708_L14_N	AE29	FMC HA 14th data channel N
J15	FMC1_HA14_P	B708_L14_P	AF28	FMC HA 14th data path P
F17	FMC1_HA15_N	B707_L6_N	AL33	FMC HA 15th data channel N
F16	FMC1_HA15_P	B707_L6_P	AL32	FMC HA 15th data path P
E16	FMC1_HA16_N	B707_L8_N	AK34	FMC HA 16th data channel N
E15	FMC1_HA16_P	B707_L8_P	AK33	FMC HA 16th data path P
K17	FMC1_HA17_CC_N	B707_L14_N	AK36	FMC HA 17th data (clock) channel N
K16	FMC1_HA17_CC_P	B707_L14_P	AL35	FMC HA 17th data (clock) P
J19	FMC1_HA18_N	B709_L0_N	AB30	FMC HA 18th data channel N
J18	FMC1_HA18_P	B709_L0_P	AB29	FMC HA 18th data path P
F20	FMC1_HA19_N	B707_L0_N	AK30	FMC HA 19th data channel N
F19	FMC1_HA19_P	B707_L0_P	AL30	FMC HA 19th data path P
E19	FMC1_HA20_N	B707_L15_N	AM37	FMC HA 20th data channel N
E18	FMC1_HA20_P	B707_L15_P	AL36	FMC HA 20th data path P
K20	FMC1_HA21_N	B706_L9_N	AP33	FMC HA 21st data channel N

Pin number	signal name	FPGA pin names	FPGA pins	Remark
K19	FMC1_HA21_P	B706_L9_P	AP32	FMC HA 21st data path P
J22	FMC1_HA22_N	B706_L10_N	AN33	FMC HA 22nd data channel N
J21	FMC1_HA22_P	B706_L10_P	AM32	FMC HA 22nd data path P
K23	FMC1_HA23_N	B706_L11_N	AM31	FMC HA 23rd data channel N
K22	FMC1_HA23_P	B706_L11_P	AN31	FMC HA 23rd channel data P
K26	FMC1_HB00_CC_N	B707_L1_N	AH29	FMC HB 0th data (clock) N
K25	FMC1_HB00_CC_P	B707_L1_P	AJ29	FMC HB Channel 0 Data (Clock) P
J25	FMC1_HB01_N	B707_L4_N	AH32	FMC HB First Channel Data N
J24	FMC1_HB01_P	B707_L4_P	AG31	FMC HB First Channel Data P
F23	FMC1_HB02_N	B707_L3_N	AJ31	FMC HB Second Channel Data N
F22	FMC1_HB02_P	B707_L3_P	AK31	FMC HB Second Channel Data P
E22	FMC1_HB03_N	B707_L2_N	AG30	FMC HB 3rd channel data N
E21	FMC1_HB03_P	B707_L2_P	AH30	FMC HB 3rd channel data P
F26	FMC1_HB04_N	B707_L5_N	AH33	FMC HB 4th data channel N
F25	FMC1_HB04_P	B707_L5_P	AJ32	FMC HB 4th data path P
E25	FMC1_HB05_N	B706_L4_N	AP35	FMC HB 5th data channel N
E24	FMC1_HB05_P	B706_L4_P	AN34	FMC HB 5th data path P
K29	FMC1_HB06_CC_N	B706_L5_N	AR35	FMC HB 6th data channel N
K28	FMC1_HB06_CC_P	B706_L5_P	AR34	FMC HB 6th data path P
J28	FMC1_HB07_N	B706_L3_N	AN37	FMC HB 7th data channel N
J27	FMC1_HB07_P	B706_L3_P	AN36	FMC HB 7th data path P
F29	FMC1_HB08_N	B706_L2_N	AR37	FMC HB 8th data channel N
F28	FMC1_HB08_P	B706_L2_P	AP36	FMC HB 8th data path P
E28	FMC1_HB09_N	B706_L1_N	AT37	FMC HB 9th data channel N
E27	FMC1_HB09_P	B706_L1_P	AT36	FMC HB 9th data path P
K32	FMC1_HB10_N	B708_L0_N	AC37	FMC HB 10th data channel N
K31	FMC1_HB10_P	B708_L0_P	AD37	FMC HB 10th data path P
J31	FMC1_HB11_N	B711_L0_N	L28	FMC HB 11th data channel N

Pin number	signal name	FPGA pin names	FPGA pins	Remark
J30	FMC1_HB11_P	B711_L0_P	M28	FMC HB 11th data path P
F32	FMC1_HB12_N	B707_L7_N	AM35	FMC HB 12th data channel N
F31	FMC1_HB12_P	B707_L7_P	AM34	FMC HB 12th data channel P
E31	FMC1_HB13_N	B706_L7_N	AU33	FMC HB 13th data channel N
E30	FMC1_HB13_P	B706_L7_P	AU32	FMC HB 13th data path P
K35	FMC1_HB14_N	B706_L15_N	AU30	FMC HB 14th data channel N
K34	FMC1_HB14_P	B706_L15_P	AU29	FMC HB 14th data path P
J34	FMC1_HB15_N	B706_L6_N	AT34	FMC HB 15th data channel N
J33	FMC1_HB15_P	B706_L6_P	AT33	FMC HB 15th data channel P
F35	FMC1_HB16_N	B711_L6_N	L32	FMC HB 16th data channel N
F34	FMC1_HB16_P	B711_L6_P	L31	FMC HB 16th data path P
E34	FMC1_HB19_N	B706_L14_N	AT31	FMC HB 1st 9th channel data N
E33	FMC1_HB19_P	B706_L14_P	AT30	FMC HB 1st 9th channel data P
D5	FMC1_GBTCLK0_M2C_C_N	104_CLK0_N	H9	Transceiver reference clock 0 input N
D4	FMC1_GBTCLK0_M2C_C_P	104_CLK0_P	J9	Transceiver reference clock 0 input P
B21	FMC1_GBTCLK1_M2C_C_N	104_CLK1_N	H11	Transceiver Reference Clock 1 Input N
B20	FMC1_GBTCLK1_M2C_C_P	104_CLK1_P	J11	Transceiver Reference Clock Input 1 P
C3	FMC1_DP0_C2M_N	105_TX3_N	E23	Transceiver data 0 output N
C2	FMC1_DP0_C2M_P	105_TX3_P	F23	Transceiver data 0 output P
C7	FMC1_DP0_M2C_N	105_RX3_N	B23	Transceiver data 0 Input N
C6	FMC1_DP0_M2C_P	105_RX3_P	C23	Transceiver data 0 Input P
A23	FMC1_DP1_C2M_N	105_TX2_N	E21	Transceiver data 1 Output N
A22	FMC1_DP1_C2M_P	105_TX2_P	F21	Transceiver Data 1 Output P
A3	FMC1_DP1_M2C_N	105_RX2_N	B21	Transceiver Data 1 Input N
A2	FMC1_DP1_M2C_P	105_RX2_P	C21	Transceiver Data 1 Input P
A27	FMC1_DP2_C2M_N	105_TX1_N	E19	Transceiver data 2 output N
A26	FMC1_DP2_C2M_P	105_TX1_P	F19	Transceiver Data 2 Output P

Pin number	signal name	FPGA pin names	FPGA pins	Remark
A7	FMC1_DP2_M2C_N	105_RX1_N	B19	Transceiver Data 2 Input N
A6	FMC1_DP2_M2C_P	105_RX1_P	C19	Transceiver Data 2 Input P
A31	FMC1_DP3_C2M_N	105_TX0_N	E17	Transceiver data 3 Output N
A30	FMC1_DP3_C2M_P	105_TX0_P	F17	Transceiver data 3 output P
A11	FMC1_DP3_M2C_N	105_RX0_N	B17	Transceiver data 3 Input N
A10	FMC1_DP3_M2C_P	105_RX0_P	C17	Transceiver data 3 Input P
A35	FMC1_DP4_C2M_N	104_TX2_N	E13	Transceiver data 4 Output N
A34	FMC1_DP4_C2M_P	104_TX2_P	F13	Transceiver data 4 output P
A15	FMC1_DP4_M2C_N	104_RX2_N	B13	Transceiver data 4 Input N
A14	FMC1_DP4_M2C_P	104_RX2_P	C13	Transceiver data 4 Input P
A39	FMC1_DP5_C2M_N	104_TX0_N	E9	Transceiver data 5 Output N
A38	FMC1_DP5_C2M_P	104_TX0_P	F9	Transceiver data 5 output P
A19	FMC1_DP5_M2C_N	104_RX0_N	B9	Transceiver data 5 Input N
A18	FMC1_DP5_M2C_P	104_RX0_P	C9	Transceiver data 5 Input P
B37	FMC1_DP6_C2M_N	104_TX1_N	E11	Transceiver data 6 Output N
B36	FMC1_DP6_C2M_P	104_TX1_P	F11	Transceiver data 6 output P
B17	FMC1_DP6_M2C_N	104_RX1_N	B11	Transceiver data 6 Input N
B16	FMC1_DP6_M2C_P	104_RX1_P	C11	Transceiver data 6 Input P
B33	FMC1_DP7_C2M_N	104_TX3_N	E15	Transceiver data 7 Output N
B32	FMC1_DP7_C2M_P	104_TX3_P	F15	Transceiver data 7 output P
B13	FMC1_DP7_M2C_N	104_RX3_N	B15	Transceiver data 7 Input N
B12	FMC1_DP7_M2C_P	104_RX3_P	C15	Transceiver data 7 Input P

Table 3.8.1 - FMC + HPC connector pin assignments

3.9 SD Card

The AXVM2152 carrier board includes a Micro SD card interface that supports the SD3.0 protocol , providing users with access to SD card storage for storing the XCVM2152 chip's boot program, Linux operating system kernel , file system, and other user data files.

SDIO signal is connected to the I/O signal of the FPGA's BANK 501 , and can accommodate

SD2.0 or SD3.0 cards; we use an NVT4857UKZ level converter for this connection. The schematic diagram of the FPGA and SD card connector is shown in Figure 3.9.1 .

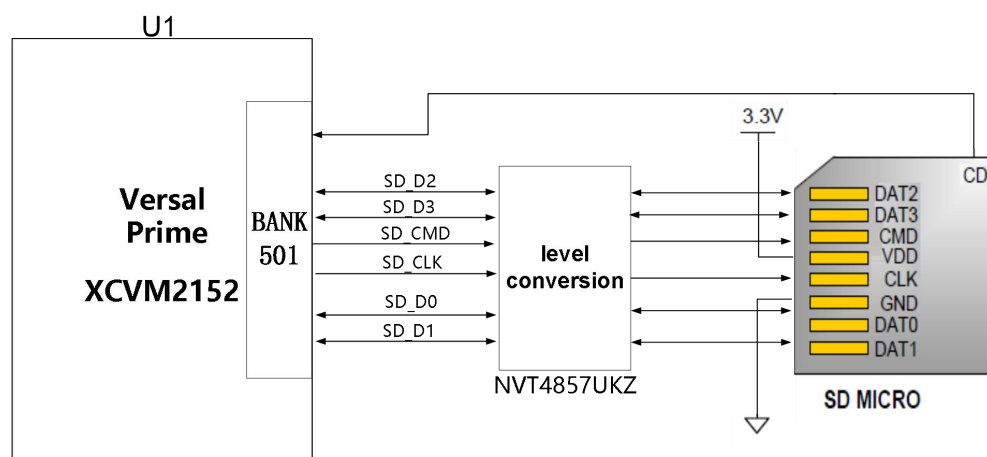


Figure 3.9.1 - SD Card Connection Diagram

SD card slot pin assignment

Signal name	Pin name	Pin number	Remark
PMC_MIO26_SD_CLK	PS_MIO26	AA8	SD clock signal
PMC_MIO28_SD_DET	PS_MIO28	AC8	SD card detection signal
PMC_MIO29_SD_CMD	PS_MIO29	AC7	SD command signals
PMC_MIO30_SD_DAT0	PS_MIO30	AB7	SD Data0
PMC_MIO31_SD_DAT1	PS_MIO31	AA7	SD Data1
PMC_MIO32_SD_DAT2	PS_MIO32	Y6	SD Data2
PMC_MIO33_SD_DAT3	PS_MIO33	AA6	SD Data3

Table 3.9.1 - SD Card Slot Pin Assignment

3.10 EEPROM and Temperature Sensor

The AXVM2152 carrier board features an EEPROM, model 24LC04, with a capacity of 4Kbit (2*256*8bit), which communicates with the PS terminal via the I2C bus. The development board incorporates a high-precision, low-power digital temperature sensor chip—the ON Semiconductor LM75—with a temperature accuracy of 0.5 degrees. The EEPROM and temperature sensor are connected to the Bank502 MIO of the Versal Prime via the I2C bus. Figure 3.10.1 shows the schematic diagram of the EEPROM and temperature sensor.

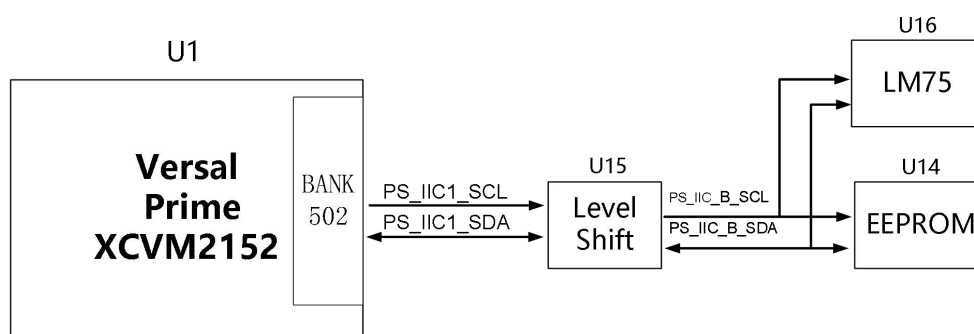


Figure 3.10.1 - Schematic diagram of EEPROM and sensor

The EEPROM communication pin assignments are as follows:

Signal name	Pin name	Pin number	Remark
PS_IIC1_SCL	LPD_MIO6	AD6	I2C clock signal
PS_IIC1_SDA	LPD_MIO7	AE6	I2C data signal

Table 3.10.1 - EEPROM Communication Pin Assignment

3.11 JTAG

The AXVM2152 development board features a JTAG interface for downloading FPGA programs and firmware to the FLASH memory. To prevent FPGA chip damage caused by live insertion or removal, a protection diode is added to the JTAG signals to maintain voltage within the FPGA's operational range. Note: Avoid hot-plugging when inserting or removing the JTAG interface.

3.12 CANFD Communication Interface

The AXVM2152 development board features two CAN/CANFD communication interfaces, connected to the MIO interface of BANK502 on the PS system side. The CANFD transceiver chip employed is NXP's TJA1051T/3/1J chip. Figure 3.12.1 shows a schematic diagram of the CAN transceiver chip connections on the PS side.

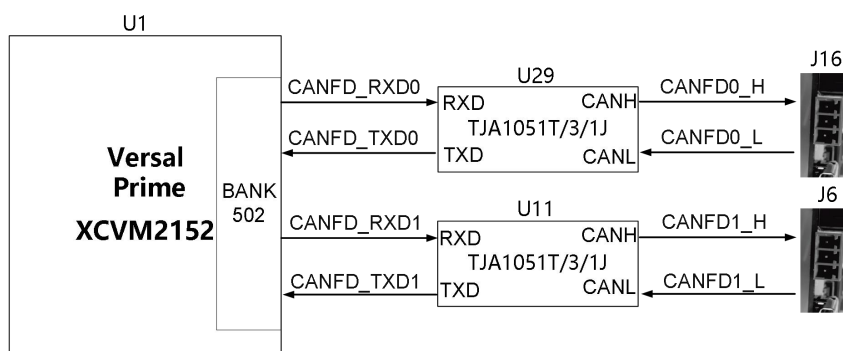


Figure 3.12.1 - Connection diagram of the PS-side CAN transceiver chip

The CAN communication pin assignments are as follows:

Signal name	pin name	pin number	Remark
CANFD_TXD0	LPD_MIO3	AG7	CAN 0 Transmitter
CANFD_RXD0	LPD_MIO2	AF8	CAN 0 receiver
CANFD_TXD1	LPD_MIO0	AD8	CAN 1 transmitter
CANFD_RXD1	LPD_MIO1	AE8	CAN 1 receiver

Table 3.12.1 - CAN Communication Pin Assignment

3.13 40-pin Expansion Port

The AXVM2152 development board reserves one 40-pin expansion header J9 with a standard 2.54mm pitch, designed for connecting external modules and devices. This expansion header provides 2 channels of 3.3V power supply, 1 channel of 5V power supply, 3 ground pins, and 34 I/O pins. The I/O pins adopt a 3.3V logic level standard. **Do not directly connect them to the I/O ports of 5V devices, otherwise the FPGA may be burned out. A level shifting chip is required if interfacing with I/O ports of 5V devices.**

J9 expansion port FPGA pin assignment

J9 number	pin	FPGA pin names	FPGA numbers	pin	J 9 pin number	FPGA pin names	FPGA numbers	pin
1		GND	-		2	+5V	-	
3		B401_L0_N	C37		4	B401_L0_P	D37	
5		B401_L1_N	C36		6	B401_L1_P	D36	
7		B401_L2_N	A36		8	B401_L2_P	B37	
9		B401_L3_N	A35		10	B401_L3_P	B35	
11		B401_L4_N	A33		12	B401_L4_P	B34	
13		B401_L5_N	C34		14	B401_L5_P	C35	
15		B401_L6_N	C31		16	B401_L6_P	C32	
17		B401_L7_N	B32		18	B401_L7_P	B33	
19		B401_L8_N	A31		20	B401_L8_P	A32	
21		B401_L9_N	A30		22	B401_L9_P	B29	
23		B401_L10_N	B30		24	B401_L10_P	C30	
25		B400_L0_N	F36		26	B400_L0_P	F37	

J9 number	pin	FPGA pin names	FPGA numbers	pin	J 9 pin number	FPGA pin names	FPGA numbers	pin
27		B400_L1_N	E36		28	B400_L1_P	F35	
29		B400_L4_N	D32		30	B400_L4_P	E33	
31		B400_L5_N	F32		32	B400_L5_P	F33	
33		B400_L8_N	C29		34	B400_L8_P	D29	
35		B400_L9_N	E29		36	B400_L9_P	F30	
37		GND	-		38	GND	-	
39		+3.3V	-		40	+3.3V	-	

Table 3.13.1 - Pin Assignments for J55 Expansion Port FPGA

3.14 Buttons

The AXVM2152 carrier board contains two user buttons, KEY1 and KEY2. Both buttons are connected to the FPGA's general-purpose I/O pins; one is connected to the PL pin, and the other to the PS pin. The buttons are active low; when a button is pressed, the FPGA's I/O input voltage is low, and when no button is pressed, the FPGA's I/O input voltage is high. The button circuit is shown in Figure 3.14.1 .

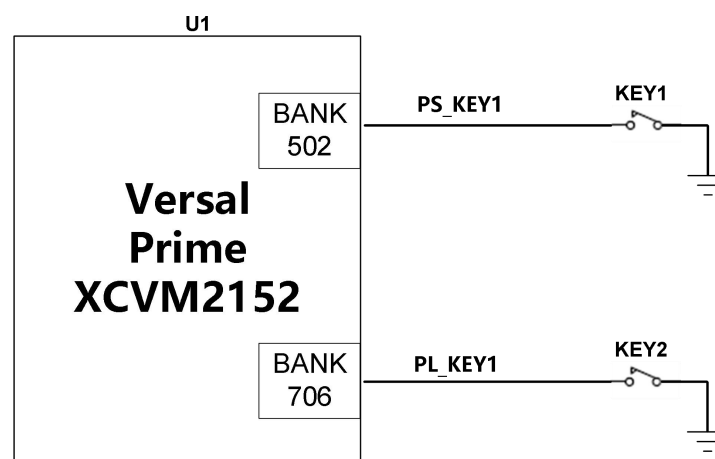


Figure 3.14.1 - Schematic diagram of button hardware design

Button FPGA Pin Assignment:

Signal name	FPGA pin names	FPGA pin numbers	Remark
PS_KEY1	LPD_MIO4	AF7	User PS terminal button
PL_KEY1	B706_L13_P	AR29	User PL terminal buttons

Table 3.14.1 - FPGA Pin Assignment for Buttons

3.15 LED

The AXVM2152 carrier board has four red LEDs: one DONE LED, one power indicator (PWR), and two user LEDs (LED1~LED2). The power indicator lights up when the development board is powered on. User LEDs 1~LED2 are connected to the FPGA's general-purpose I/O pins; one is connected to the PL pin, and the other to the PS pin. When the I/O voltage connected to the user LED is configured to a high level, the user LED lights up; when the I/O voltage is configured to a low level, the user LED is turned off. The schematic diagram of the LED hardware connection is shown in Figure 3.15.1 .

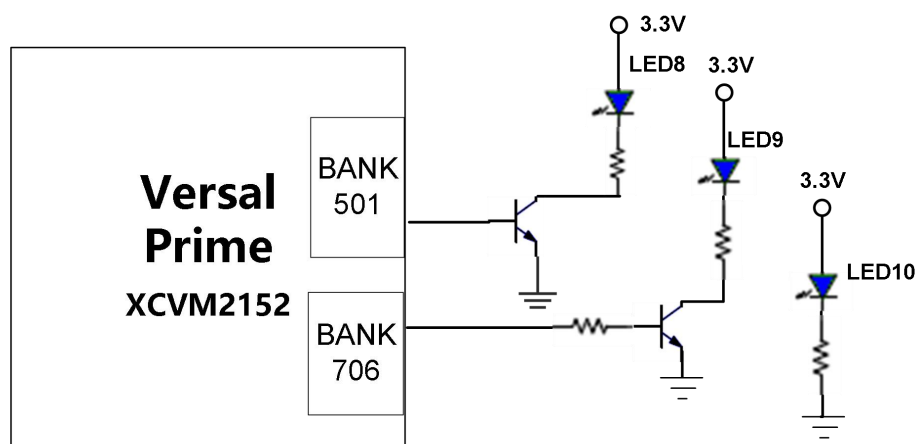


Figure 3.15.1 - Schematic diagram of LED lamp hardware design

LED FPGA pin assignment:

Signal name	FPGA pin names	FPGA pin numbers	Remark
PS_LED1	PS_MIO51	W1	PS User-defined indicator light
PL_LED1	B706_L13_N	AP30	PL user-defined indicator lights

Table 3.15.1 - LED FPGA Pin Assignment

3.16 Power Supply

The input power voltage of the AXVM2152 carrier board is DC 12V. Please use the original power adapter supplied with the development board. Do not use power supplies of other specifications to avoid damaging the board. On the carrier board, four DC/DC power chips convert the input voltage into four power rails: +5V, +3.3V, +1.8V and +1.2V. In addition, the +12V power supply on the carrier board feeds power to the som through a board-to-board connector. The power supply design of the expansion board is shown in Figure 3.16.1 below: .

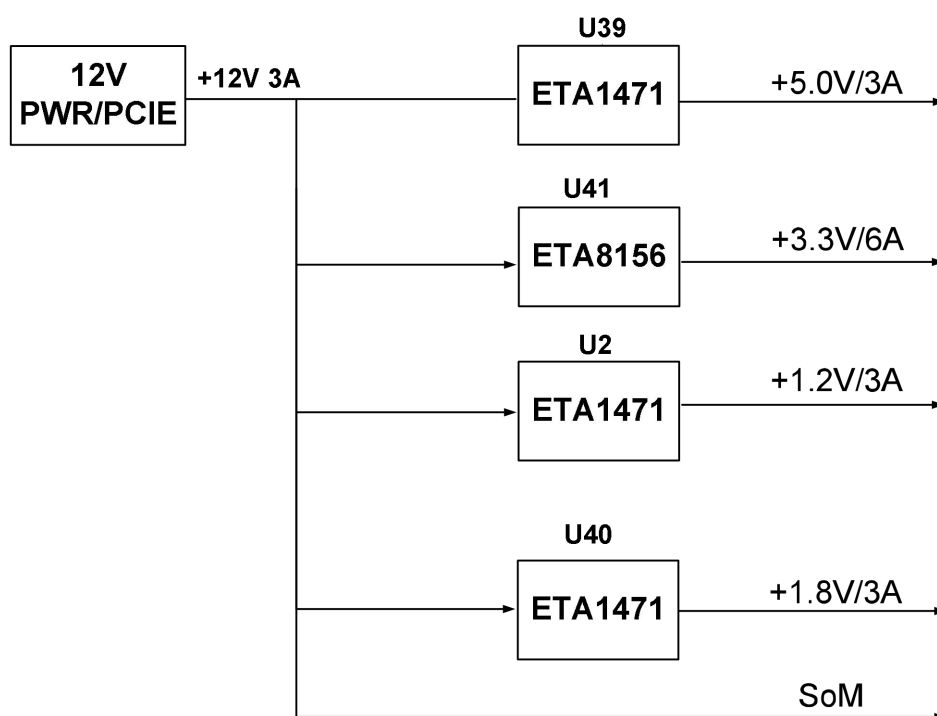


Figure 3.16.1 - Power supply schematic of expansion board

3.17 Structural Dimensions Drawing

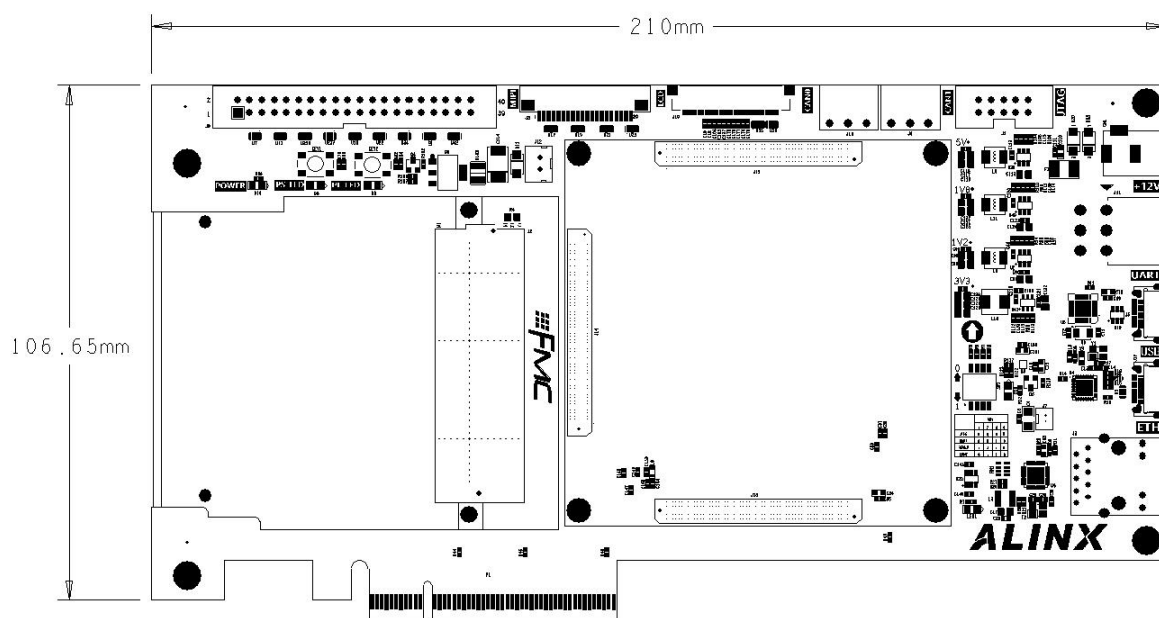


Figure 3.17.1 - Top View



Alinx Electronic Limited

Company Website: www.en.alinx.com

Service Hotline: 021-67676997

Technical Support : technical@alinx.com

